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(Ultra)wide bandgap semiconductor heterostructures for electronics cooling

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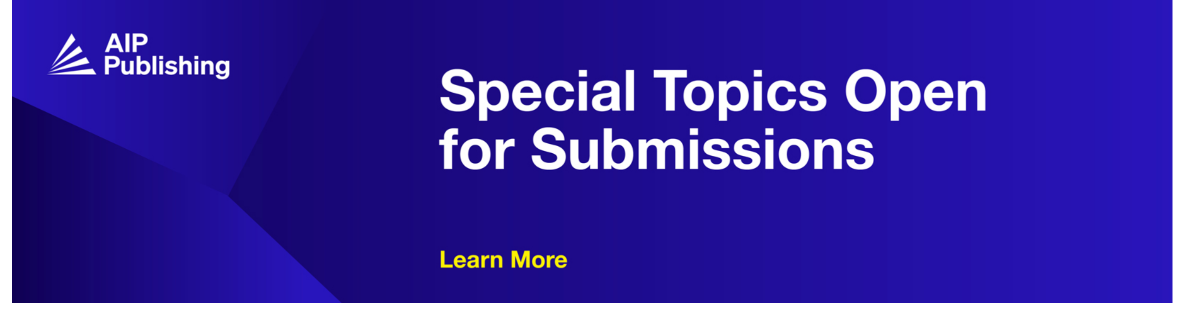

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(Ultra)wide bandgap semiconductor heterostructures for electronics cooling

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ABSTRACT

The evolution of power and radiofrequency electronics enters a new era with (ultra)wide bandgap semiconductors such as GaN, SiC, and β-Ga_2O_3, driving significant advancements across various technologies. The elevated breakdown voltage and minimal on-resistance result in size-compact and energy-efficient devices. However, effective thermal management poses a critical challenge, particularly when pushing devices to operate at their electronic limits for maximum output power. To address these thermal hurdles, comprehensive studies into thermal conduction within semiconductor heterostructures are essential. This review offers a comprehensive overview of recent progress in (ultra) wide bandgap semiconductor heterostructures dedicated to electronics cooling and are structured into four sections. Part 1 summarizes the material growth and thermal properties of (ultra)wide bandgap semiconductor heterostructures. Part 2 discusses heterogeneous integration techniques and thermal boundary conductance (TBC) of the bonded interfaces. Part 3 focuses on the research of TBC, including the progress in thermal characterization, experimental and theoretical enhancement, and the fundamental understanding of TBC. Parts 4 shifts the focus to electronic devices, presenting research on the cooling effects of these heterostructures through simulations and experiments. Finally, this review also identifies objectives, challenges, and potential avenues for future research. It aims to drive progress in electronics cooling through novel materials development, innovative integration techniques, new device designs, and advanced thermal characterization. Addressing these challenges and fostering continued progress hold the promise of realizing high-performance, high output power, and highly reliable electronics operating at the electronic limits.

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I. INTRODUCTION

Compared to Si, (ultra)wide bandgap semiconductors, such as GaN, SiC, and β-Ga_2O_3, exhibit higher breakdown voltage and lower specific on-resistance, resulting in the creation of more compact and efficient devices.[1] For instance, to block the same voltage, GaN and β-Ga_2O_3 require only 9% and 4% of Si material, respectively.[1,2] The Baliga figure of merits (BFOM) of GaN and β-Ga_2O_3, which measures the minimized resistive losses, are 870 and 2870 times of Si, respectively.[1,2]

These semiconductors hold immense promise in power electronics and radiofrequency (RF) electronics, ushering in revolutionary applications such as radar systems, satellite communication, 5G stations, renewable energy, electric vehicles, energy infrastructures, and consumer electronics.[1,3] However, the Joule heating in these devices generates localized hot spots, elevating device temperature and subsequently compromising performance and reliability. Consequently, thermal management poses significant challenges in the electro-thermal co-design of (ultra)wide bandgap electronics. Furthermore, as the devices become increasingly compact, highly integrated, and high-performance, the challenges of heat dissipation become increasingly serious.

Addressing the heat spreading of localized hotspots within electronic devices necessitates a keen focus on the thermal resistances of semiconductor heterostructures, comprising thin films and interfaces. The quality of grown crystals plays a pivotal role in determining thermal conductivity and in turn, impacts the heat dissipation of electronics. Table I provides a summary of the bandgap and intrinsic thermal conductivity of bulk (ultra)wide bandgap semiconductors at room temperature, with Si included for comparison. The intrinsic thermal conductivity serves as the upper limit of the semiconductor, while the thermal conductivities of corresponding thin films are all reduced due to boundary and defect scatterings of phonons.

After several decades of development, GaN electronics have carved out a distinctive niche in high-power and high-frequency applications. However, thermal limitations have emerged as a major impediment in realizing the maximum output power from GaN transistors operating near the electronic limit of the material. The hot spots in AlGaN/GaN high-electron mobility transistors (HEMTs) possess extremely small sizes (tens of nanometers) and can exhibit extremely high heat flux (even one order of magnitude higher than that of the Sun's surface), underscoring the critical role of heat spreading in thermal design to mitigate peak temperatures. Moreover, the median lifetime of GaN devices declines by half with every 10 °C increase in channel temperature.[18] Consequently, today's GaN electronics are constrained by thermal considerations, prompting ongoing research efforts to overcome these limitations.[18] The thermal properties within the semiconductor heterostructures are pivotal for thermal management, emphasizing the desirability of high thermal conductivity films and interfaces with elevated thermal boundary conductance (TBC).

Another wide bandgap semiconductor, SiC, exhibits significant potential in high-power electronic devices and has been widely used in electric vehicles.[19] Distinctive thermal properties have been observed in both 4H-SiC and 6H-SiC, which demonstrate thermal conductivities in the range of 300–400 W m^{-1} K^{-1} as shown in Table I. Recent research has also unveiled a record-high thermal conductivity for wafer-scale high-quality 3C-SiC,[7] which holds the highest electron mobility among all SiC polytypes, suggesting further opportunities for

TABLE I. Summary of bandgap, thermal conductivity, and heat capacity of (ultra)wide bandgap semiconductors at room temperature.[4–17] Si is also added for comparison.

Material	Band gap/eV	Thermal conductivity (W m^{-1} K^{-1})	Heat capacity (MJ m^{-3} K^{-1})	Type
GaN	3.4	220	2.63	
4H-SiC	3.3	345(out plane), 415(in plane)	2.12	Wide
6H-SiC	3.0	320(out plane), 390(in plane)	2.17	Bandgap
3C-SiC	2.3	500	2.14	
β-Ga_2O_3	4.8	27([010]), 11([100])	2.82	Ultrawide
Diamond	5.5	2200	1.75	
AlN	6.2	321	2.44	Bandgap
$Al_xGa_{(1-x)}N$	3.4–6.2	25–115	⋯	
Si	1.1	142	1.63	

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the application of high-performance power devices based on 3C-SiC even though it has relatively small bandgap.

Recently, the ultrawide bandgap semiconductor β-Ga_2O_3 has garnered significant attention due to advances in growth techniques that make large-scale wafer production from melt-grown crystals potentially affordable.[2,3,20] β-Ga_2O_3 even exhibits a higher BFOM than GaN, with corresponding device demonstrations showing excellent performance.[3,21] However, the intrinsic thermal conductivity of β-Ga_2O_3 is highly anisotropic and at least one order of magnitude lower than that of the other (ultra)wide bandgap semiconductors.[8,15,22] Moreover, the thermal conductivity of β-Ga_2O_3 nanostructures is further reduced significantly due to size effects.[22–24] As such, overheating problems in β-Ga_2O_3 electronics represent one of the two main challenges for real-world applications, the other being *p*-type doping.[3] Heterogeneous integration of β-Ga_2O_3 electronics with other high thermal conductivity materials is a possible way to cool these electronics.

Except for β-Ga_2O_3, AlN, which has an ultrawide bandgap, has found extensive use in the field of optoelectronic devices, including deep ultraviolet (DUV) LEDs.[26,27] However, these devices grapple with the issue of overheating, as a substantial portion of the energy is converted into heat.[26] With recent advances to the *p*-doping problem,[27] it is anticipated that there will be an upsurge in AlN electronic and optoelectronic applications, underscoring the significance of enhancing the thermal performance of AlN devices.

This review provides a comprehensive overview of recent advances in the field of (ultra)wide bandgap semiconductor heterostructures for applications of thermal management of electronics. Specifically, it encompasses recent developments in four key areas: (1) Materials growth involving the production of high-quality (ultra)wide bandgap semiconductor crystals and heterostructures with enhanced thermal conductivity; (2) heterogeneous integration strategies for (ultra)wide bandgap semiconductors aimed at electronics cooling; (3) advanced thermal metrology techniques for characterizing the TBC of (ultra) wide bandgap semiconductor heterostructures, experimental and theoretical techniques for enhancing TBC of interfaces as well as the fundamental understanding of TBC, which highlights the recent discovery of localized phonon modes at interfaces; and (4) simulation studies investigating temperature distribution in devices and assessing the efficacy of various cooling methods and evaluation of the practical impact of heterostructures on device cooling and temperature measurement techniques; Fig. 1 shows the motivation and focus of this review. By scrutinizing the state-of-the-art experiment and theory, the aim is to identify key challenges that exist in the cooling of (ultra)wide bandgap electronics and propose potential future research directions to overcome these challenges. This article aims to provide valuable insights

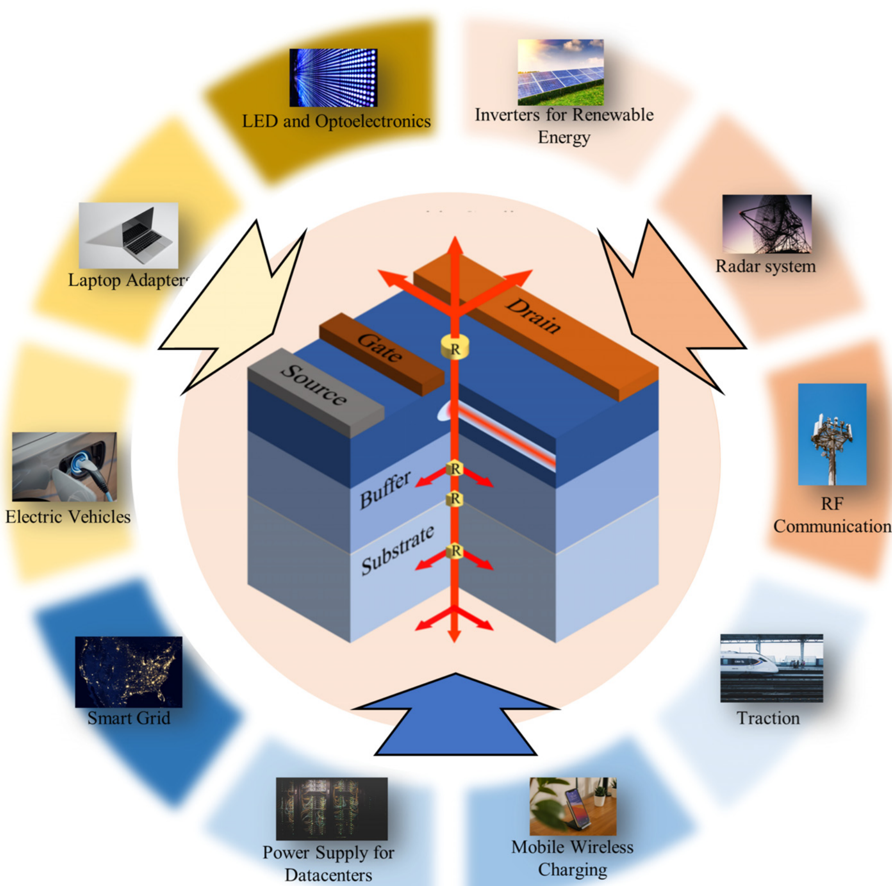

FIG. 1. Motivation and focus of this review.

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for researchers and engineers in the field of (ultra)wide bandgap semiconductors.

II. MATERIALS GROWTH: HIGH QUALITY ACHIEVING HIGH THERMAL CONDUCTIVITY

The growth of high-quality and pure materials is essential for achieving high thermal conductivity. Figure 2 provides a summary of the state-of-the-art measured thermal conductivity and wafer size of high thermal conductivity materials.[7] Currently, (ultra)wide bandgap semiconductor materials, including GaN, SiC, diamond, and AlN, can be grown at large wafer size with high thermal conductivity. Although some boron compounds have high thermal conductivity, their mm-scale or smaller crystal size hinders them from being scaled up for massive production and widespread adoption.

The measured thermal conductivity of most (ultra)wide bandgap semiconductors, such as diamond, GaN, 4H-SiC, and 6H-SiC, has reached the intrinsic high values predicted by density functional theory (DFT). This achievement can be attributed to the availability of large wafers with exceptional crystal quality and purity, which eliminate phonon-boundary and phonon-defect scatterings.[1,6,7] Notably, the measured thermal conductivity of AlN and 3C-SiC has traditionally fallen below the theoretically predicted values. Recent collaborative efforts among researchers in thermal science and material growth, pushing the boundaries of crystal quality and purity, have experimentally observed the intrinsic high thermal conductivity of AlN and 3C-SiC wafers.[7,10]

A. GaN growth

Recently, high-quality GaN layers have been laterally overgrown on the mask-patterned sapphire and Si substrates using halide vapor phase epitaxy (HVPE), resulting in a significantly reduced amount of dislocations. The high quality of GaN crystal even grown on foreign substrates has enabled a record-high critical electric field, which approaches the theoretical limit of GaN.[38] Additionally, HVPE has successfully produced high-purity *n*-GaN layers with the highest reported electron mobility at room temperature.[39] In addition, by utilizing MgO as Mg doping source, *p*-type GaN was also fabricated successfully by applying HVPE,[40,41] which also lead to the first demonstration of *p-n* junction GaN.[42] While no experimental measurements have been reported yet, it is anticipated that high-purity GaN crystals will exhibit high thermal conductivity.

For efficient near-junction heat spreading of GaN electronics, it is preferred to use diamond as the substrate since single-crystal diamond has the highest thermal conductivity among natural materials. However, mismatches in lattices and thermal expansion coefficients between GaN and diamond pose challenges for direct high-quality epitaxial growth of GaN on diamond or vice versa. Polycrystalline diamond, grown on GaN crystals with nanoscale diamond seeds and SiN_x or AlN dielectric protective layers at the interfacial regions, exhibits orders of magnitude lower thermal conductivity compared to single-crystal diamond. Moreover, the protective layers introduce additional thermal resistance, limiting the cooling performance of GaN-on-diamond devices.

Epitaxial growth of GaN on single-crystal diamond has shown some progress, as depicted in Fig. 3. By incorporating physical vapor deposited (PVD) AlN and graphene on a diamond substrate, a second layer of AlN is grown on top as a transition layer. Subsequent growth of GaN on the AlN transition layer leads to the formation of a uniformly distributed single-crystal continuous film, as shown in Figs. 3(a) and 3(b).[39] However, the additional PVD layer, graphene layer, and corresponding interfaces create significant thermal resistance between the high-quality GaN region and the single-crystal diamond substrate. Furthermore, the GaN layer may exfoliate from the diamond substrate due to the van der Waals interfaces of graphene, posing challenges for device fabrication.

An alternative technique to grow GaN on a single-crystal diamond without graphene involves the growth of multiple AlN and AlGaN transition layers to alleviate stress and lattice mismatch, as illustrated in Figs. 3(c) and 3(d).[43] The orientation of the used diamond substrate is (111). However, obtaining large-area single diamonds with (111) orientation poses a significant challenge. Moreover, AlGaN exhibits low thermal conductivity due to alloy scatterings of phonons. The transition layers and interfaces also create large thermal resistances between GaN and diamond. Unfortunately, the thermal properties of structures grown using these two techniques remain unmeasured, emphasizing the necessity for further studies in both thermal characterizations and the fabrication of practical electronic devices based on these epitaxial layers.

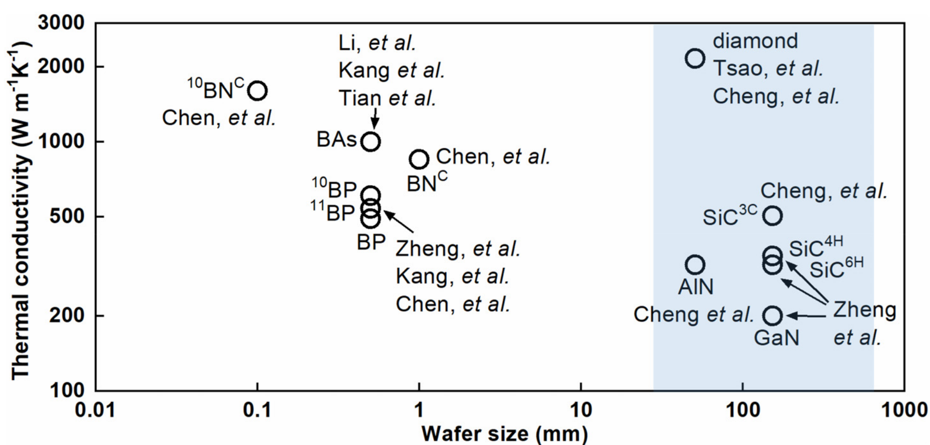

FIG. 2. State-of-the-art thermal conductivity values and wafer sizes of high thermal conductivity semiconductors.[1,6,7,10,28–37] Reprinted with permission from Cheng *et al.*, Nat. Commun. **13**, 7201 (2022). Copyright 2022 Springer Nature.[7]

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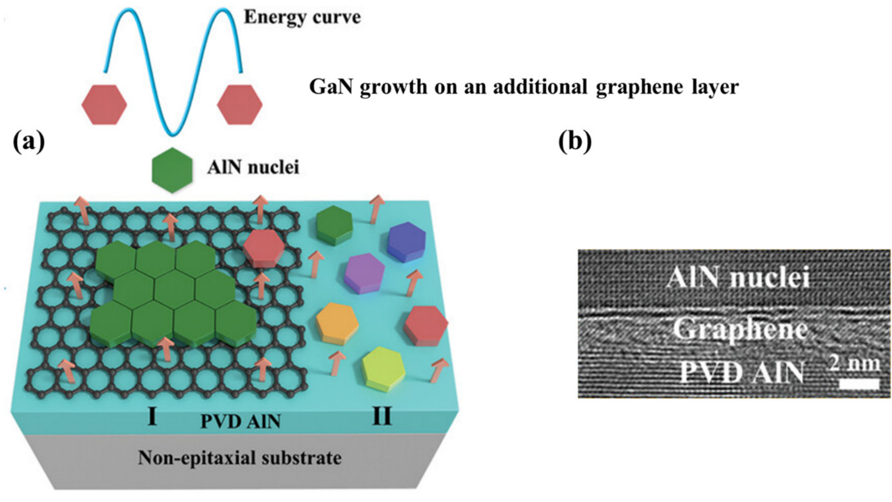

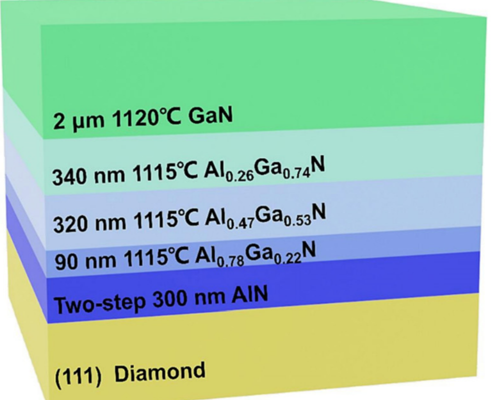

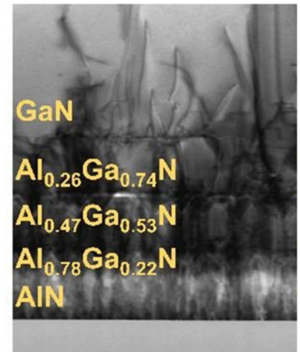

FIG. 3. Methods for GaN growth on diamond substrates. (a) With an additional graphene layer and a PVD AlN layer underneath, the AlN and GaN can be grown on the diamond substrate in fixed in-plane orientation and the GaN layer becomes a uniformly distributed single-crystal continuous film. Reprinted with permission from Liu *et al.*, Adv. Funct. Mater. **32**, 2113211 (2022). Copyright 2022 Wiley-VCH.[44] (b) GaN growth on diamond substrates through series of buffer layers Reprinted with permission from Gao *et al.*, Mater. Des. **235**, 112444 (2023). Copyright 2023 Elsevier.[44]

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B. β-Ga_2O_3 growth

β-Ga_2O_3 boasts an ultrawide bandgap of almost 4.6–4.9 eV, contributing to its high critical electric field.[3] The most advantageous feature of β-Ga_2O_3 is its sizable, scalable, and potentially cost-effective substrate. Moreover, β-Ga_2O_3 can be *n*-type doped to achieve a low resistivity of approximately 1 mΩ·cm.[46] The challenge of introducing a *p*-type component may potentially be addressed through integration with heterojunctions, a concept encouraged by the recent demonstration of *p*-NiO/*n*-Ga_2O_3 *p*-*n* heterojunctions with avalanche robustness.[46] This unique combination of large-size bulk availability and doping feasibility has sparked significant interest in the rapidly growing field of power electronics.

In contrast to other ultrawide bandgap semiconductors, single-crystal gallium oxide can be grown using the melt method, which eliminates the need for extreme growth pressure. Since Ga_2O_3 features multiple polymorphs, the growth of other polymorphs of Ga_2O_3 also attracts numerous research interest.[47] The primary challenge of β-Ga_2O_3 lies in its low and anisotropic thermal conductivity, leading to severe overheating issues in power devices. This intrinsic limitation in thermal conductivity, governed by intrinsic phonon properties, cannot be improved by growing high-quality crystals. As a potential solution, the epitaxial growth of β-Ga_2O_3 thin films on high thermal conductivity materials such as SiC and diamond emerges as a promising approach to mitigate overheating problems in β-Ga_2O_3 devices.[48–52]

C. AlN growth

AlN stands out as a promising ultrawide bandgap semiconductor with wide-ranging applications in electronics and optoelectronics due to the large bandgap and high critical electric field.[27] Notably, recent advancements include substantial bulk *p*-type doping of AlN using beryllium, as well as a dopant-free AlN-based p-n junction diode, thereby elevating AlN to the status of a genuine semiconductor[27,53]

Bulk AlN wafers are typically grown by the physical vapor transport (PVT) technique. Second ion mass spectroscopy (SIMS) measurements reveal that there exist high concentrations (10^{19} atoms per cm^3) of impurities such as carbon, oxygen, and silicon in bulk AlN wafers, as illustrated in Fig. 4(a).[10] Recent developments in the epitaxial

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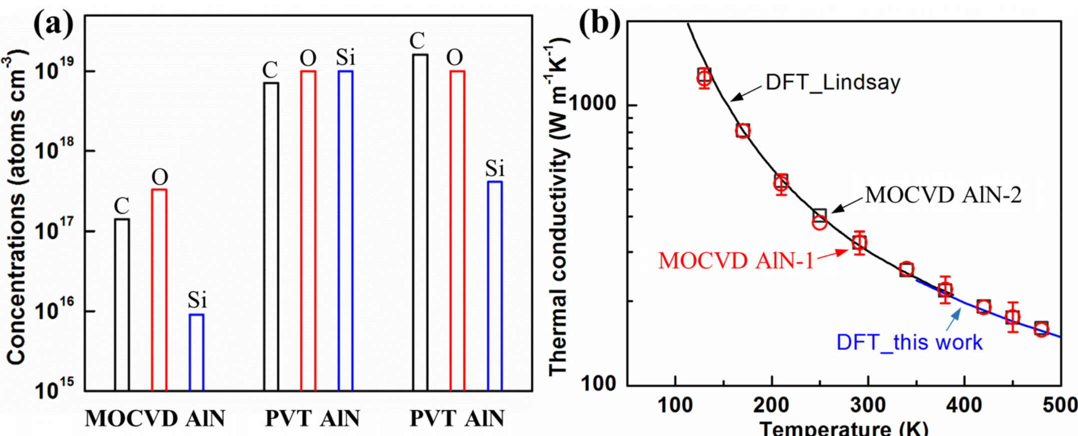

FIG. 4. Intrinsic high thermal conductivity of AlN. (a) SIMS data of impurity concentrations in MOCVD AlN and PVT AlN.[10] (b) Temperature-dependent thermal conductivity of high-quality MOCVD AlN. The experimentally measured thermal conductivity matches well with DFT-calculated values of single-crystal AlN. Reprinted with permission from Cheng *et al.*, Phys. Rev. Mater. **4**, 044602 (2020). Copyright 2020 American Physical Society.[10]

growth of thick AlN crystals on sapphire substrates via metal-organic chemical vapor deposition (MOCVD) have yielded crystals with high purity. This improved purity in AlN contributes to a substantial increase in thermal conductivity, reaching 321 W m^{-1} K^{-1} at room temperature, as depicted in Fig. 4(b).[10] Significantly, the measured cross-plane thermal conductivity of high-purity AlN grown by MOCVD aligns excellently with theoretical values calculated for single-crystal AlN using DFT. The dislocation densities of both samples are not high enough to affect the cross-plane thermal conductivity but may have an impact on the in-plane thermal conductivity.[10,54,55] Due to the hetero-epitaxial growth, the MOCVD-grown AlN on sapphire has a higher density of dislocations than the bulk AlN crystals grown by PVT.

To further enhance the quality of AlN, there is a renewed focus on selective area growth, a traditional growth technology renowned for its efficacy in producing high-quality crystal thin films.[56] This approach seeks to achieve a low dislocation density, comparable to that found in native bulk substrates. In the case of AlN, the selective area growth of AlN islands is meticulously controlled to facilitate coalescence without the formation of new threading dislocations (TDs) after coalescence, utilizing nano-patterned sapphire substrates, as illustrated in Fig. 5.

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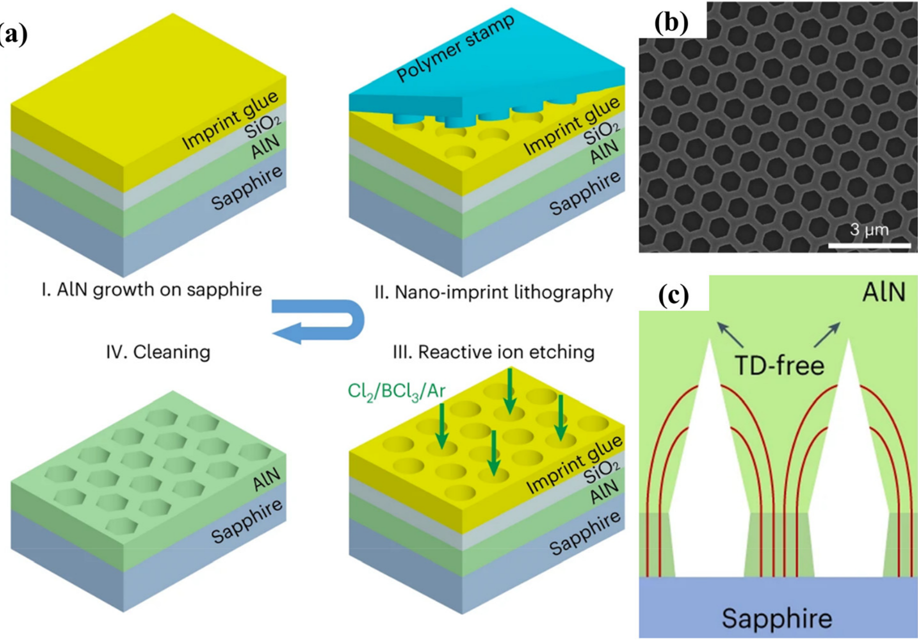

FIG. 5. Selective area growth of high-quality AlN (AlN film growth on NPATs). (a) The fabrication of NPATs. (b) The TEM image of the surface of NPATs with periodic hexagonal holes. (c) The evaluation of TDs in AlN films grown on NPATs. Reprinted with permission from Wang *et al.*, Nat. Mater. **22**, 853 (2023). Copyright 2023 Springer Nature.[56]

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The fabrication of nano-patterned AlN/sapphire templates (NPATs) involves the use of reactive ion etching (RIE) to etch the AlN layer grown on sapphire with the aid of nano-imprint lithography. A transmission electron microscope (TEM) is employed to scrutinize the surface structure. The periodic hexagonal holes in the substrates reduce the density of threading dislocations (TDs) significantly, resulting in high-quality AlN.[5] The thermal conductivity of the high-quality AlN would further approach the theoretical values, especially for the in-plane thermal conductivity, which are impacted strongly by the density of dislocations.

Emerging cooling techniques such as top-side cooling involve the deposition of materials with high thermal conductivity onto electronic device surfaces, which limits the deposition temperature to be lower than 400 °C. However, the synthesis of high-quality crystals that have superior thermal conductivity typically necessitates high-temperature conditions. Consequently, there is a growing demand for high thermal conductivity dielectric materials that can be deposited at low temperatures. Figure 6(a) illustrates a schematic diagram of the growth of crystalline AlN via sputtering at room temperature.[6] Remarkably, the polycrystalline AlN thin films demonstrate thermal conductivities surpassing 100 W m^{-1} K^{-1}, as evidenced in Fig. 6(b). Figure 6(b) also encapsulates a comparison of deposition temperatures against the thermal conductivity of various high thermal conductivity materials. A notable trend is observed: as deposition temperatures decrease, crystal quality diminishes, leading to a corresponding reduction in thermal conductivity. Within the constraints of back-end-of-line (BEOL) compatible temperatures, AlN exhibits the highest thermal conductivity within sub-micrometer thickness ranges.

D. Digital alloys and superlattices

The growth of AlN/GaN and β-Ga_2O_3/Al_2O_3 alloys and superlattices can be precisely controlled in chemical vapor deposition (CVD) or molecular beam epitaxy (MBE) growth processes. Figure 6 illustrates the successful growth of single monolayer (ML) AlN and GaN. Due to the absence of crystal symmetry, the atoms forming the atomic layer in two opposite directions parallel to certain crystal axes have different sequences. GaN, AlN, and their ternary alloys exhibit spontaneous polarization, leading to polarization-induced fixed charges and mobile carriers at the heterointerface, commonly known as a two-dimensional electron gas (2DEG) or two-dimensional hole gas (2DHG).[58] If these heterointerfaces are densely aligned, as seen in atomically thin superlattices composed of alternating layers of AlN and GaN, known as digital alloys (DAs), there might be an overlap of the 2DEG across layers, resulting in an extended carrier distribution. Notably, electrons in such atomically ordered compounds, like superlattices, do not experience alloy scattering. Consequently, these superlattices could provide a practical way to enhance the mobility of AlGaN, particularly at an Al composition where impurity doping is ineffective.

Structured digital alloys show significant promise for improving the performance of light-emitting diodes and power electronics.[5] Furthermore, in the case of a compositional graded AlGaN, the distribution gradient of the polarization field can generate fixed charges and mobile carriers (occasionally addressed as three-dimensional electron gas or hole gas), such bulk doping methodology, referred to as distributed polarization doping (DPD), is characterized by its impurity-free feature which does not require thermally ionization energy.[59] This impurity-free feature is a promising approach for doping ultrawide bandgap materials like AlN and high Al-content AlGaN, addressing challenges posed by deep impurity levels. Recently, Wang *et al.* reported the discovery of superlattices between GaN and Mg, referred to as Mg-intercalated GaN superlattices (MiGs).[60] They achieved this by depositing a metallic Mg thin film onto bulk single-crystal GaN, followed by annealing the sample under atmospheric pressure. This straightforward and accessible process leads to the diffusion of Mg atoms into the GaN substrate as single-atomic layers. The incorporation of Mg induces significant variations in the GaN lattice constant and introduces considerable strain within the structure, potentially increasing the thermal conductivity, which requires further investigation. *P*-type GaN can be easily achieved by optimizing the annealing temperature.

Contrary to their electrical properties, digital alloys and superlattices exhibit a strong reduction in thermal conductivity due to alloy scattering and boundary scatterings of phonons. Figures 7(a), 7(b), and 7(e) depict recent progress in the growth of ultrathin layers of GaN or

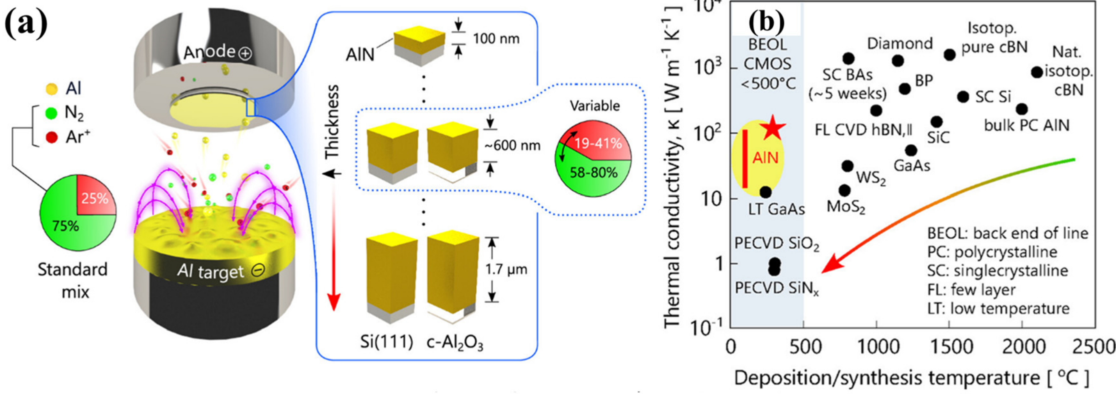

FIG. 6. AlN growth at low temperature.[57] (a) The schematic diagram of the sputtering of the AlN thin layer at room temperature. (b) The deposition temperature and thermal conductivity of high thermal conductivity materials. Reprinted with permission from Perez *et al.*, ACS Nano **17**, 21240 (2023). Copyright 2023 American Chemical Society.[57]

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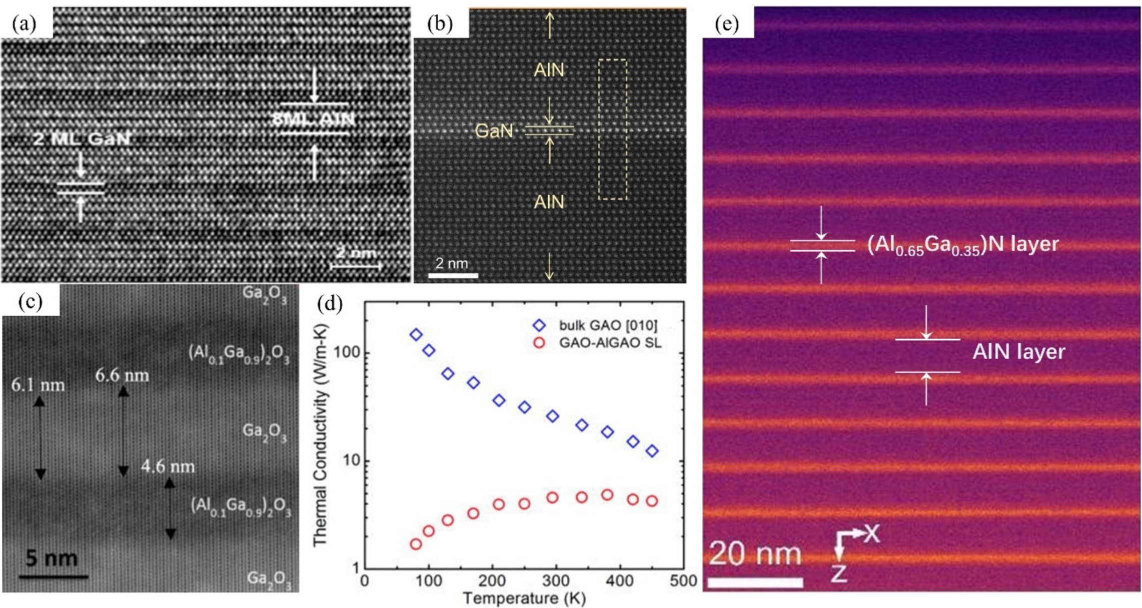

FIG. 7. Digital alloys and superlattices of AlN and GaN, β-Ga_2O_3, and Al_2O_3. (a) The cross-sectional TEM images of digital alloyed $(AlN)_8/(GaN)_2$ structure growth by metal-organic vapor phase epitaxy method. Reprinted with permission from Gao *et al.*, Cryst. Growth Des. **19**, 1720 (2019). Copyright 2019 American Chemical Society.[61] (b) A monolayer of GaN grown between AlN layers on the c-plane. Reprinted with permission from Wu *et al.*, Proc. Natl. Acad. Sci. U. S. A. **120**, e2303473120 (2023). Copyright 2023 National Academy of Sciences.[62] (c) and (d) The high-angle annular dark field-scanning transmission electron microscopy (HAADF-STEM) image of a β-$(Al_{0.1}Ga_{0.9})_2O_3/Ga_2O_3$ superlattice structure and its thermal conductivity compared to the bulk β-Ga_2O_3 as functions of temperature. Reprinted with permission from Cheng *et al.*, Appl. Phys. Lett. **115**, 092105 (2019). Copyright 2019 AIP Publishing LLC.[22] (e) The HAADF image of an AlN-$(Al_{0.65}Ga_{0.35})N$ superlattice structure. Reprinted with permission from Hoglund *et al.*, Adv. Mater. **36**, 2402925 (2024). Copyright 2024 John Wiley and Sons.[63]

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AlGaN down to one or two monolayers. Furthermore, thermal studies are necessary to understand thermal transport in these new structures. Figure 7(d) demonstrates the measured thermal conductivity of β-$(Al_{0.1}Ga_{0.9})_2O_3/Ga_2O_3$ superlattice, which is approximately five times lower than that of the corresponding bulk crystal.[22] The layered structure of digital alloy and superlattices displays anisotropic thermal conductivity, with in-plane thermal conductivity significantly higher than cross-plane thermal conductivity.

Recently, the incorporation of scandium (Sc) has significantly increased the spontaneous polarization of AlN, propelling AlN/AlScN heterostructures to the forefront of research.[64] Additionally, other elements are proving to be influential within this context. Examples include AlPN/GaN,[65] AlBN/AlN,[66] and quinary AlScYLaN/AlN heterostructures.[67] B enhances the dielectric constant of AlN, while Sc, Y, and La boost its ferroelectric properties. Thus, the alloying of AlN with these elements offers extensive opportunities to modulate its electrical properties, unlocking the vast potential of AlN-based heterostructure systems. However, a drawback is that thermal conductivity tends to diminish with the introduction of additional alloying elements, potentially leading to overheating issues in electronic applications.

The adjustment of a certain component's composition can result in variations in the phonon properties of the structure. In a recent study, the proportions of Ga and Al or Ga and In in the alloy $In_xGa_{1-x}N$ or $Al_xGa_{1-x}N$ were modified.[68] The fraction x ranged from 5% to 20%, and this material served as an interlayer between Al and GaN. By controlling the composition of Al or In atoms, the impact on TBC was investigated, as depicted in Fig. 8. Figure 8(a) presents a TEM image of the fabricated interface, clearly illustrating the presence of an interlayer. The TBC values observed under various compositions are shown in Fig. 8(b). However, the discernible effect of composition on the TBC of this structure warrants further investigation.

E. SiC growth

Silicon carbide has about 250 crystalline polytypes. The 4H-SiC and 6H-SiC have been widely applied in power electronics as active components or substrate materials. The commercially available high-quality wafers have achieved intrinsic high thermal conductivity which agrees with first-principal calculations.[6,36,37] The massive production also leads to stable crystalline quality of wafers up to 8 in. size. The large wafer size facilitates cost reduction in related electronics. Due to the expensive cost of ultrahigh purity SiC, smart-cut techniques have been developed to bond high-purity SiC on low-quality SiC substrates to form composite wafers. Most studies focus on homo-epitaxy since hetero-epitaxy of 4H-SiC and 6H-SiC are still challenging. The effects of structural imperfections such as defects or dislocations on thermal conductivity are much less studied than those on electrical properties. The understanding of defect–phonon scattering and electron–phonon scattering in 4H-SiC and 6H-SiC crystalline is still very limited.[69]

The cubic phase of silicon carbide (3C-SiC) has been less explored experimentally, compared to its hexagonal counterparts, namely, 4H-SiC and 6H-SiC, primarily due to the scarcity of high-quality and pure wafers. Recent theoretical calculations suggest that the 3C-SiC has the highest intrinsic thermal conductivity among all

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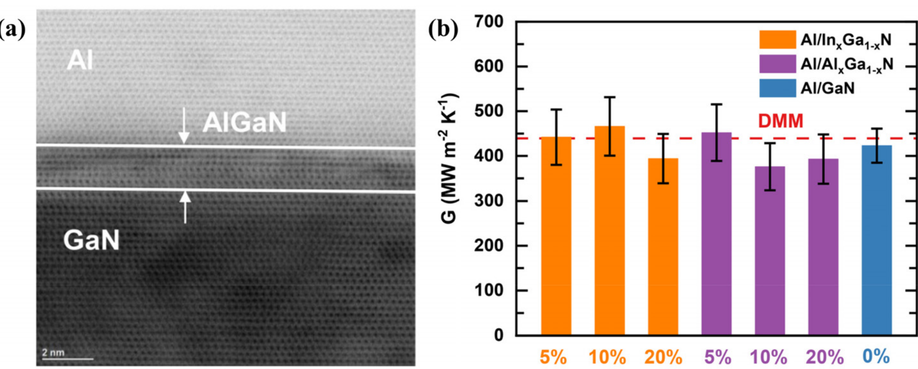

FIG. 8. The regulation of the material composition of the interlayer. (a) The TEM image of the GaN/Al interface and the $Al_xGa_{1-x}N$ interlayer. (b) TBCs of different interlayers of different material compositions. Reprinted with permission from Li *et al.*, J. Appl. Phys. **134**, 230901 (2023). Copyright 2023 AIP Publishing LLC.[68]

SiC polytypes (exceeding 500 W m^{-1} K^{-1}). However, historically, the measured thermal conductivity in the literature was about 50% lower than the theoretical predictions.[70] This discrepancy was attributed to the presence of impurities or grain boundaries within the studied 3C-SiC crystals.[70] In particular, boron impurities was identified as potent phonon scatterers, significantly diminishing thermal conductivity beyond even the effects of vacancies.[70]

High-purity and high-quality 3C-SiC crystals have recently been demonstrated to have a high thermal conductivity exceeding 500 W m^{-1} K^{-1}.[71] Figure 9(a) presents the picture of high-quality and high-purity 3C-SiC wafer grown by CVD in a customized chamber.[7] The freestanding 3C-SiC single-crystal wafer is fabricated by initially growing a thick layer on a silicon substrate, followed by subsequent removal of the substrate through etching.[7] The measured thermal conductivity

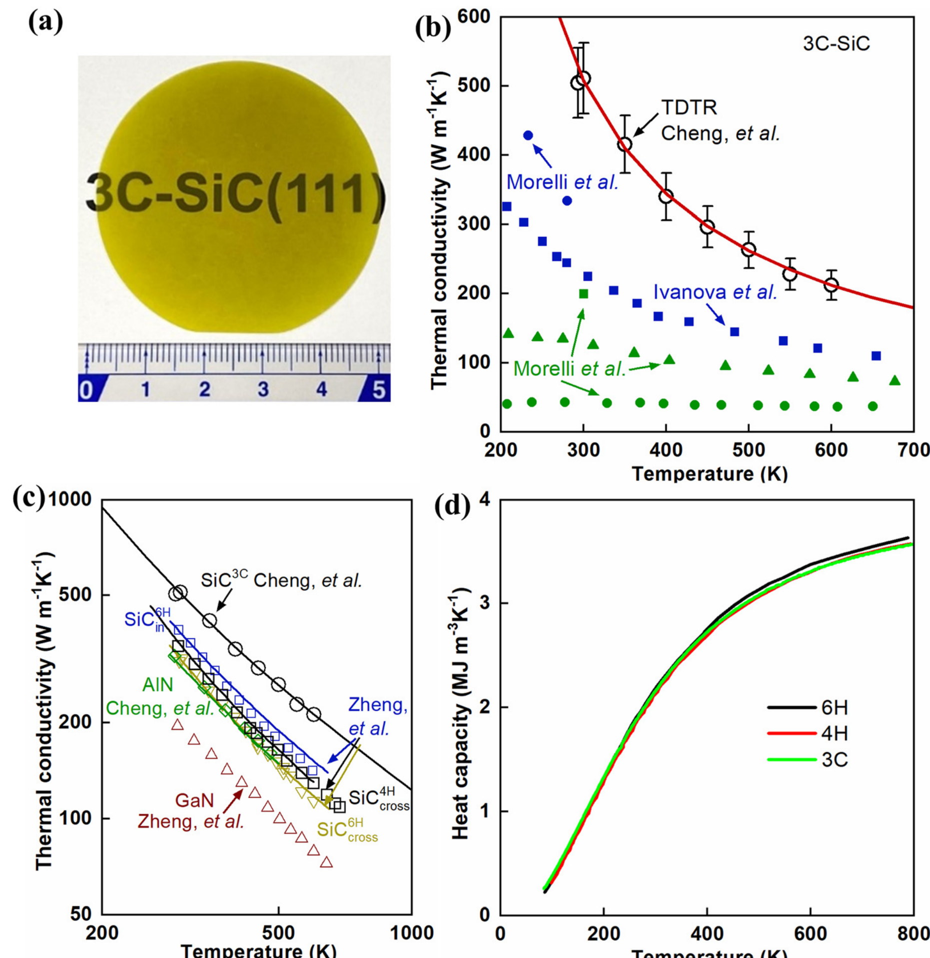

FIG. 9. High thermal conductivity of wafer-scale 3C-SiC crystals. (a) Picture of a 3C-SiC freestanding wafer.[7] (b) Experimentally measured high thermal conductivity of high-quality 3C-SiC matches well with DFT-predicted values of single-crystal 3C-SiC.[7] The literature data of measured thermal conductivity of 3C-SiC is also included for comparison.[72,73] (c) The isotropic thermal conductivity of 3C-SiC is compared with other high thermal conductivity wafers (AlN, GaN, 4H-SiC, and 6H-SiC).[6,7,10,74] Both the in-plane and cross-plane thermal conductivity of 6H-SiC are included since it is anisotropic.[6] (d) Suggested data of volumetric heat capacity of 3C-SiC, 4H-SiC, and 6H-SiC.[6,7] Reprinted with permission from Cheng *et al.*, Nat. Commun. **13**, 7201 (2022). Copyright 2022 Springer Nature.[7]

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of the high-quality and high-purity 3C-SiC closely aligns with theoretical predictions and markedly surpasses previously documented values, as depicted in Fig. 9(b).[7] Notably, the thermal conductivity of 3C-SiC ranks second only to diamond among large crystals; however, diamond's applications are hindered by its limited wafer size alongside its exorbitant cost and the challenges associated with semiconductor integration. In contrast, 3C-SiC can grow large wafers up to 8 in., which is important for massive production. Figure 9(c) illustrates the superior temperature-dependent thermal conductivity of 3C-SiC relative to 4H-SiC, 6H-SiC, GaN, and AlN single crystals across the measured temperatures.[7] Additionally, due to its cubic structure, 3C-SiC exhibits isotropic thermal properties, maintaining high thermal conductivity in both in-plane and cross-plane orientations. Moreover, there is a close concordance with minimal deviations observed in heat capacity data among 4H-SiC, 6H-SiC, and 3C-SiC, as demonstrated in Fig. 9(d).[6,7]

Figure 10(a) delineates the contribution of phonons with different mean free paths (MFP) to the thermal conductivity of thin films normalized by their corresponding bulk counterparts.[7] Owing to the typically long phonon mean free paths in high thermal conductivity semiconductors, a pronounced size effect on the thermal conductivity of these thin films is anticipated. As integral elements of functional devices, the thermal conductivity of semiconductor thin films is of paramount importance. Figures 10(b) and 10(c) depict the thickness-dependent in-plane and cross-plane thermal conductivity of semiconductor thin films.[7] The data indicate that all examined (ultra)wide bandgap semiconductor thin films exhibit a significant dependence on film thickness regarding thermal conductivity. Notably, the measured thermal conductivity values of 3C-SiC thin films reach unprecedented high values in both in-plane and cross-plane dimensions, surpassing those of CVD diamond films of comparable thicknesses. Whereas the CVD diamond films formed on dissimilar substrates are polycrystalline or nanocrystalline, the AlN, GaN, and 3C-SiC thin films approach single-crystal quality. This highlights the grain boundaries within diamond films as contributors to phonon scattering, which moreover

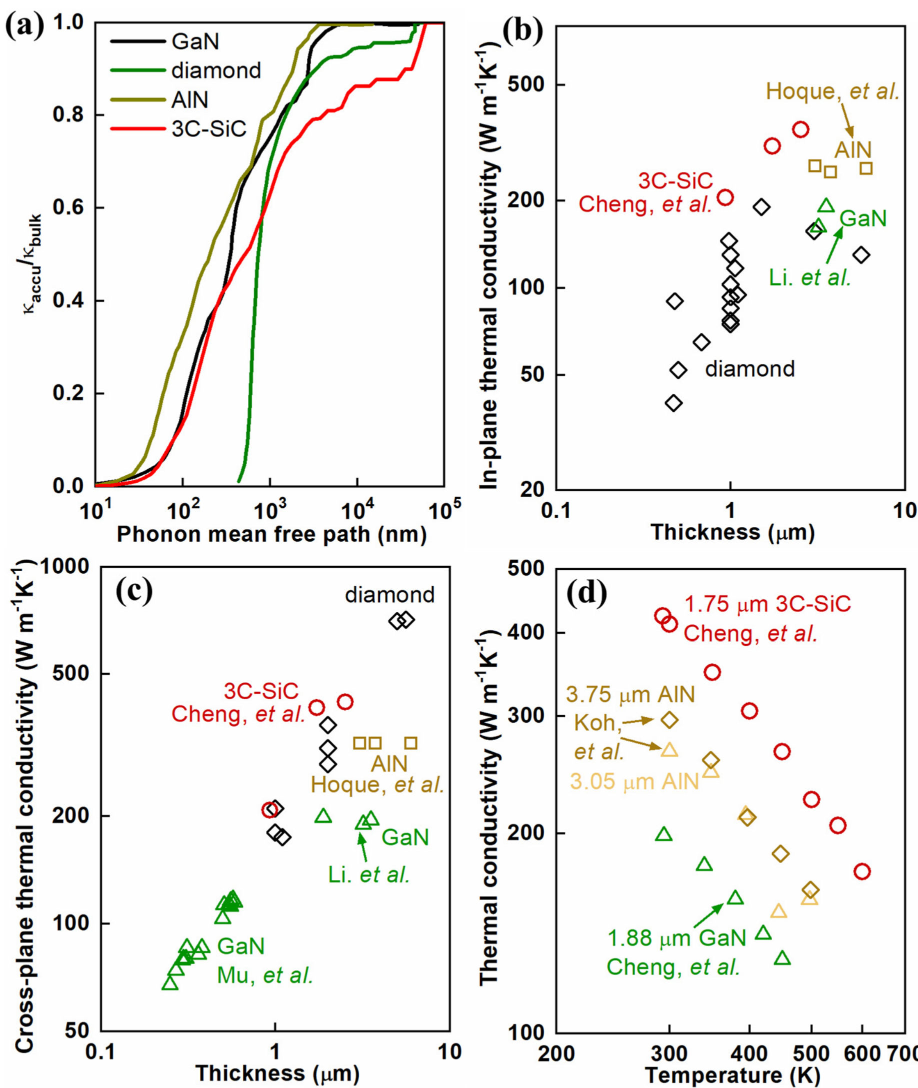

FIG. 10. Thermal conductivity of wafer-scale thin films of high thermal conductivity materials. (a) Accumulated thermal conductivity of GaN, diamond, AlN, and 3C-SiC normalized by their corresponding bulk thermal conductivity.[7] (b) Thickness-dependent in-plane thermal conductivity of thin films.[7,54,76–82] (c) Thickness-dependent cross-plane thermal conductivity of thin films.[54,76,81–85] (d) Temperature dependence of cross-plane thermal conductivity of thin films.[7,55,86] Reprinted with permission from Cheng *et al.*, Nat. Commun. **13**, 7201 (2022). Copyright 2022 Springer Nature.[7]

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reduces the thermal conductivity. As illustrated in Fig. 10(d), the cross-plane thermal conductivity of thin films still exhibits a strong temperature dependence, with 3C-SiC outperforming other semiconductors across the observed temperature range.[7] Furthermore, 3C-SiC thin films can serve as substrates or transition layers for epitaxial growth of other semiconductors, such as AlN and GaN, given that 3C-SiC is the sole SiC polytype compatible with epitaxy on Si.[75] This compatibility also renders 3C-SiC-Si composite wafers a cost-effective alternative to bare SiC wafers.

Crystals of 3C-SiC grown using CVD exhibit high thermal conductivity; however, their growth rate remained low, challenging the production of thick wafers. Recently, notable advancements have been achieved in the bulk synthesis of 3C-SiC atop 4H-SiC substrates,[87] as evidenced by Fig. 11. Optimizing nitrogen partial pressure above 15 kPa during the top-seated solution growth (TSSG) process has led to a favorable change in interfacial energies, thereby enhancing the formation of 3C-SiC compared to 4H-SiC. Such conditions facilitate the increased nucleation of 3C-SiC on the 4H-SiC seed surface and bolster the step-flow growth rate. These improvements not only promote the predominance of 3C-SiC crystal growth but also achieve high crystal quality and elevated growth rates. Figures 11(b)–11(e) display images of the resulting bulk single crystals of 3C-SiC. Although heavy nitrogen doping—at a scale of $10^{20}\,cm^{-3}$—is essential for the crystallization process, it is noteworthy that such doping may considerably compromise thermal conductivity.

III. HETEROGENEOUS INTEGRATION: BONDING WITH HIGH THERMAL CONDUCTIVITY MATERIALS

Despite significant strides in materials growth techniques leading to enhanced thermal conductivity, the demand for improved cooling solutions persists in device applications. Simply enhancing the quality of semiconductor materials falls short in adequately addressing the escalating thermal challenges confronting current and future semiconductor devices. In response to these limitations, semiconductor bonding techniques present effective solutions by capitalizing on the unique advantages of individual materials. Strategic bonding of two materials or wafers enables the full exploitation of their respective merits. Heterogeneous bonding emerges as a critical approach to harnessing the high thermal conductivity of materials such as SiC and diamond, as elaborated in Sec. II. In bonded structures, the thermal boundary conductance (TBC) between materials becomes a pivotal factor governing the extraction and dissipation of generated Joule heat, particularly in addressing hot spots.[4,88–91] Achieving a sufficiently high TBC, closely linked to the crystal structure near the interface and interlayer between materials, proves essential for successful thermal management during wafer bonding.[4,91–94] The interface structure intricately depends

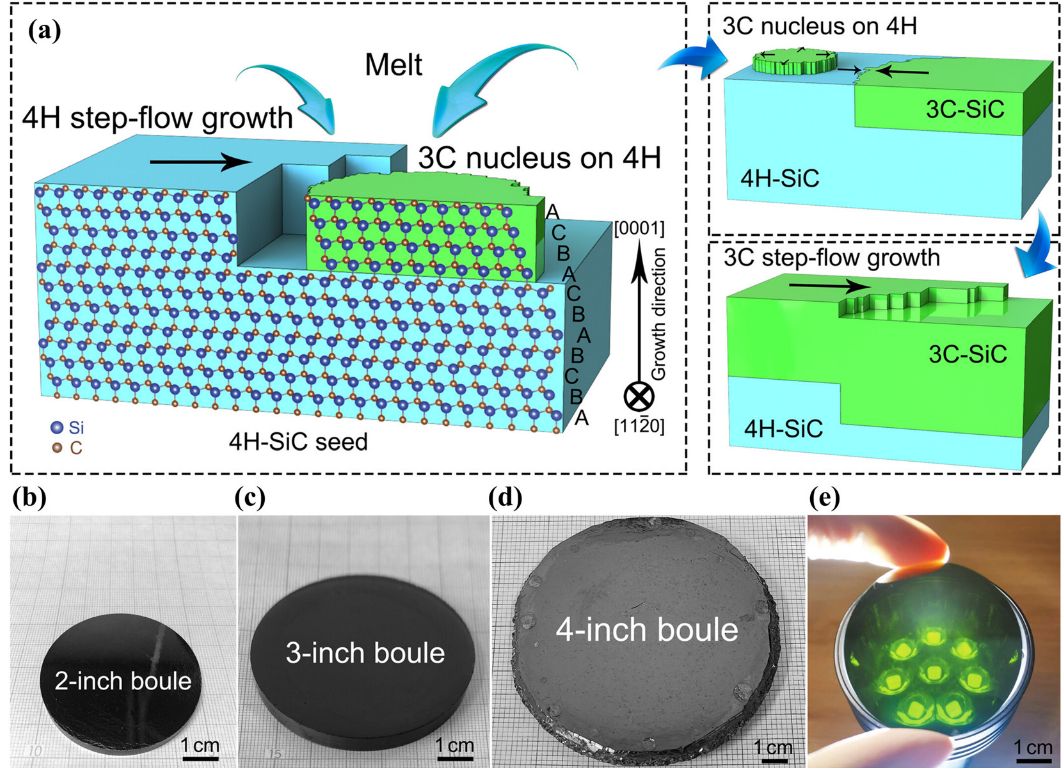

FIG. 11. The process of 3C-SiC growth on the 4H-SiC seed by TSSG method.[87] (a) 3C-SiC nucleus on 4H-SiC seed while 4H-SiC is growing. However, more 3C-SiC nuclei on 4H-SiC seed overtake the growth under appropriate N_2 partial pressure. At last, the whole surface is covered by 3C-SiC. (b) and (c) The 2- and 3-in. 3C-SiC boule obtained by TSSG followed by rounded cutting. (d) The as-growth 4 in. 3C-SiC boule. (e) 3C-SiC single-crystal wafer showed green under strong light. Reprinted with permission from Wang *et al.*, Energy Environ. Mater. **7**, e12678 (2023). Copyright 2023 Wiley.[6]

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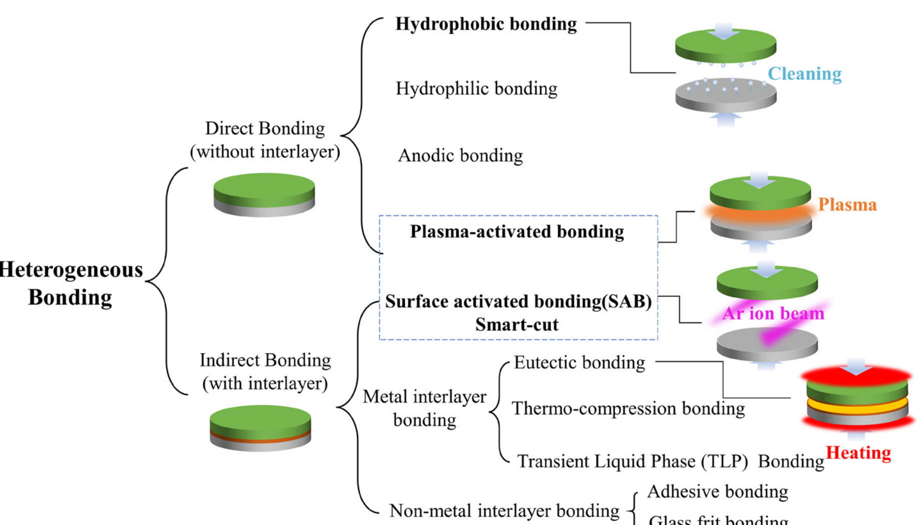

FIG. 12. The classification of different wafer bonding methods.

on the bonding methods forming the interface and subsequent post-processing steps like annealing.[86,89,95] Conventional bonding methods fall into two categories: direct bonding, where no intentional interlayer is deposited between wafers before bonding, and indirect bonding, where an interlayer is deposited to enhance bonding or offer protection. A comprehensive classification is provided in Fig. 12. Notably, plasma bonding, surface-activated bonding (SAB), and smart-cut techniques can function as either direct or indirect bonding methods, depending on specific scenarios. This review primarily delves into hydrophilic bonding, plasma bonding, surface-activated bonding (SAB), and smart-cut techniques, commonly employed in (ultra)wide bandgap semiconductors.

A. Surface-activated bonding

The surface-activated bonding (SAB) technique has attracted considerable attention in recent years amidst the increasing demand for heterogeneous integration. SAB, conducted at or near room temperature, effectively mitigates thermal stress near the bonding interface arising from mismatches in the coefficient of thermal expansion (CTE) between materials.[96] We will describe the SAB process and showcase notable examples of wafer bonding achieved through SAB in recent years.

In the preparatory stage of SAB, the two wafers intended for bonding undergo chemical–mechanical polishing (CMP) to attain a surface roughness below 0.5 nm root mean square (RMS), a critical prerequisite for the subsequent bonding process. Following this, fast Ar ions are implanted onto the bonding surfaces to further eradicate surface contaminations and native oxide layers, ensuring an atomically clean surface to achieve sufficient bonding strength.[97] The two wafers are then brought together under pressure, as depicted in Fig. 13(a), whereby the dangling bonds generated during surface activation form chemical bonds to facilitate bonding, as illustrated in Fig. 13(b). All procedures are conducted at room temperature within a high vacuum environment. Although a thin layer near the bonding interface may incur damage from the Ar ion implantation, such effects can be mitigated through post-bonding annealing.

Thanks to advancements in GaN growth technology, as discussed in Sec. II, and the refinement of device fabrication processes, GaN-based RF devices become ubiquitous in RF applications.[98,99] However, the high heat flux within the channel of GaN devices has significantly elevated the junction temperature, leading to increased instability in device performance and lifespan.[18] Therefore, integrating high thermal conductivity single-crystal diamond substrates with GaN devices has been proposed as an effective means to achieve near-junction cooling of GaN devices.[100,101] Utilizing the SAB method, GaN–diamond interfaces with high TBC can be achieved to fully exploit the advantages of diamond substrates. To ensure a strong and robust GaN–diamond interfaces, a layer of adhesion material is often applied before the bonding process. However, such layers may result in decreased TBC, as depicted in Figs. 14(a)–14(f).

In Fig. 14(a), both GaN and diamond wafers are pre-coated with an ultra-thin layer of Si to enhance bonding strength. However, this results in a thick interlayer of amorphous Si, significantly hindering heat transport across the interface.[102] Notably, a thin layer of diamond near the bonding interface turns into amorphous carbon due to Ar activation, while the GaN crystal structure remains intact. In contrast, Cheng *et al.* introduced Si into the Ar ion source, enabling simultaneous surface activation and Si interlayer deposition, resulting in a thin interlayer (only 4.2 nm) and a substantial increase in TBC, as shown in Fig. 14(b).[86] Comparatively, separately depositing Si would result in a thicker interlayer, as demonstrated in Fig. 14(c). Recently, new hybrid ion source of SiO_x contained Ar has also been adapted by Xu *et al.*, achieving an even thinner interlayer with a TBC as high as 120 MW m^{-2} K^{-1}.[103] The TBC in this study is highly sensitive to the thickness of the interlayer, which cannot be fully explained by the additional thermal resistance of the interlayer. Subsequent nonequilibrium molecular dynamics (NEMD) studies suggest that this is due to the mismatch of vibrational density of states (vDOS) between the mixture layer and the diamond or SiO_x layer.[103]

The absence of intentionally applied adhesion layers can lead to a thin amorphous interlayer, reducible through post-annealing, as depicted in Fig. 14(d).[89] Liang *et al.*, employing SAB, directly bonded a GaN layer onto a diamond substrate with an as-bonded interlayer of

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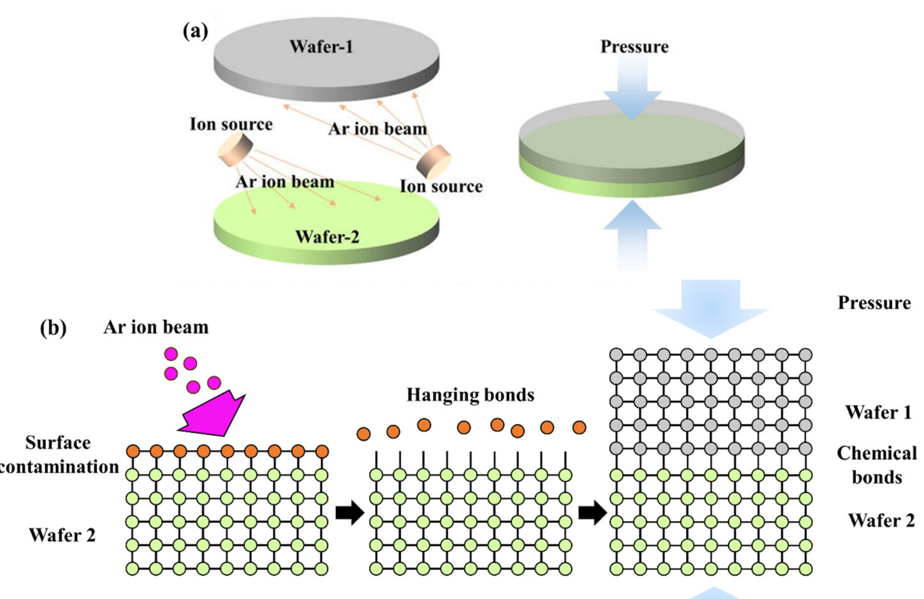

FIG. 13. The procedure and principle of SAB. (a) The macroscopic procedure of SAB, including Ar ion implantation and the bonding of two wafers. Reprinted with permission from Cheng *et al.*, Appl. Phys. Lett. **120**, 030501 (2022). Copyright 2022 AIP Publishing LLC.[90] (b) The microcosmic principle of SAB. Dangling bonds created by the implantation of Ar ions form new chemical bonds under pressure near room temperature.

5.3 nm, reduced to 1.5 nm via 1000 °C annealing. Additionally, materials other than Si can serve as interlayers. For instance, Ayaka Kobayashi *et al.* deposited a SiC layer onto the diamond surface to reduce roughness,[104] shown in Fig. 14(e). Notably, after annealing, interlayer thickness may slightly increase due to the formation of extra SiC from Si and C atoms. Ar irradiation onto a Si substrate deposits an adhesion layer of only 1.5 nm onto the diamond surface, facilitating the achievement of an ultra-thin interlayer without the need for post-annealing, as shown in Fig. 14(f).[105] While the thermal properties of this structure remain unstudied, a large TBC is anticipated.

In addition to GaN/diamond interfaces, this review provides insights into several (ultra)wide bandgap semiconductor interfaces obtained through SAB, as depicted in Figs. 15–17, encompassing GaN/Si, GaN/SiC, SiC/SiC, 3C-SiC/diamond, 4H-SiC/diamond, Si/diamond, 3C-SiC/β-Ga_2O_3, and AlN/Si interfaces.

Considering that 3C-SiC possesses a coefficient of thermal expansion (CTE) between that of diamond and GaN, along with a lattice constant close to that of GaN, and high thermal conductivity, Ryo Kagawa *et al.* utilized a 3C-SiC layer to construct a GaN/3C-SiC/diamond multilayer via SAB, buffering potential mismatches and stresses at the GaN/diamond bonding interface.[97] The as-bonded and post-annealed interfaces at 1100 °C are depicted in Figs. 15(a) and 15(b), indicating that annealing significantly improves interfacial structure, reduces amorphous interlayer thickness, and enhances TBC, which is vital for device cooling. Another bonding of SiC and GaN wafers was performed by Mu *et al.* via SAB.[85] A significant increase in TBC and interlayer recrystallization were observed after annealing at 1273 K, as shown in Fig. 15(c).

In a recent study, Ma *et al.* demonstrated a homogeneous interface composed of 4H-SiC through SAB, which is shown in Fig. 15(d).[106] Post-annealing at 1973 K yielded an interface with a high TBC, suggesting great potential for SiC-based high-power devices.[109] A thick protective layer (10 nm Ti) was applied on the diamond interface to prevent damage from Ar ion beams by Minoura *et al.*[107] The image of the interface, depicted in Fig. 15(e), suggests the formation of a 4 nm thick amorphous SiC layer created by Ar ion implantation, while preserving the diamond's crystal structure under the Ti layer. The SiC wafer was then bonded to the bottom of an AlGaN/GaN HEMT via SAB. Though the electrical performance of the HEMT improved, the TBC of the SiC/diamond interface was only 19 MW m^{-2} K^{-1}, possibly due to thick and amorphous interlayers. β-Ga_2O_3, another important ultrawide bandgap semiconductor with low thermal conductivity, can also benefit from bonding. Liang *et al.* transferred a high thermal conductivity 3C-SiC thin film onto a β-Ga_2O_3 substrate and bonded them together via SAB.[108] TEM images of the bonded interface after 1000 °C annealing, as shown in Fig. 15(f), indicate reduced amorphous interlayer thickness due to recrystallization.

Recently, Cheng *et al.* reported that post-annealing facilitates TBC enhancement by chemical reaction at the interfaces.[110] TEM and FFT images of the bonded interface after annealing at different temperatures, as shown in Fig. 16(a), indicate chemical reaction of amorphous silicon with diamond to form SiC. The transition from SiC/Si/diamond into SiC/diamond leads to a record-high TBC enhancement for all bonded and grown interfaces after annealing. The bonded SiC/diamond TBC achieves a record-high value of 150 MW m^{-2} K^{-1} among all bonded diamond interfaces. The significantly increased TBCs after high-temperature annealing are illustrated in Fig. 16(b).

The schematic diagram of a modified SAB technique and additional bonded (ultra)wide bandgap semiconductor interfaces are shown in Fig. 17. Suga *et al.* employed a novel method of depositing Si interlayer by bombarding a Si target, depositing 10 nm thick Si layers onto both SiC wafers, followed by surface activation and pressing, as shown in Fig. 17(a).[111] The as-bonded interface, depicted in Fig. 17(b), shows a thick interlayer of amorphous Si. However, after annealing at 1273 K, the interlayer is reduced to 8 nm (half of the original value), as

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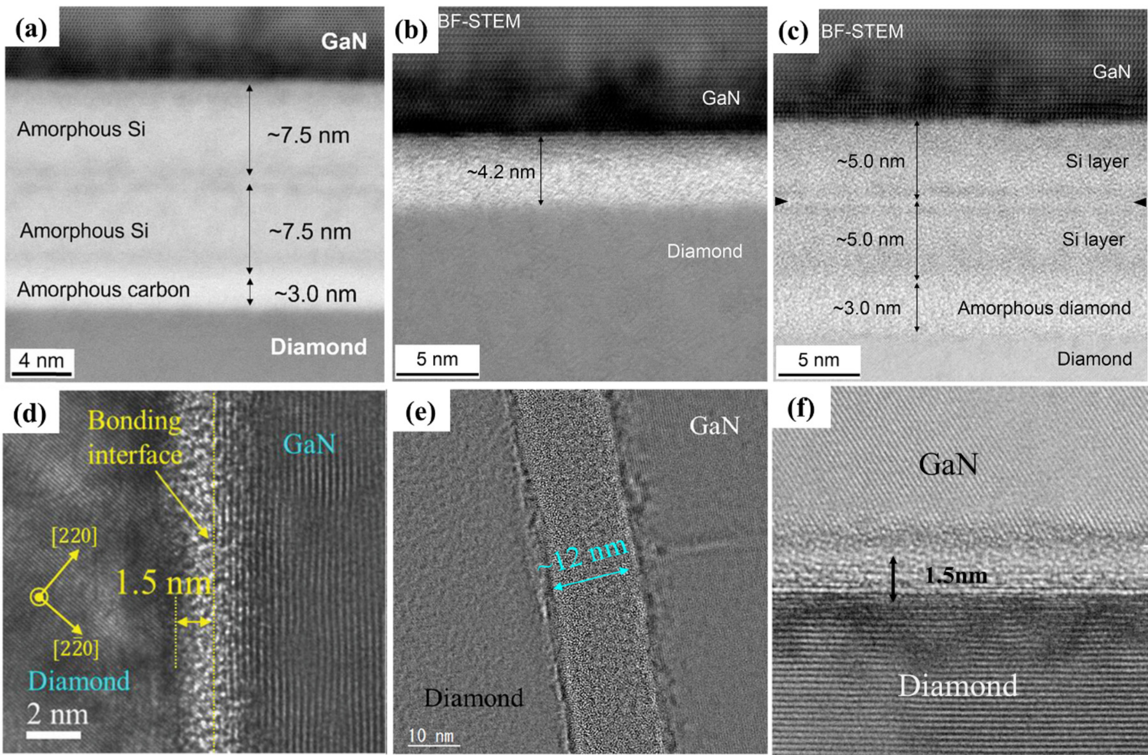

FIG. 14. The GaN/diamond interfaces bonded by SAB. (a) the image of a GaN/diamond heterointerface with a ~15-nm-thick Si interlayer to enhance the bonding strength. Reprinted with permission from Mu *et al.*, J. Alloys Compd. **905**, 164076 (2022). Copyright 2022 Elsevier BV.[102] (b) The cross-sectional image of the GaN/diamond heterointerface with a thin interlayer obtained by Si-containing Ar ion beam. (c) The cross-section image of the GaN/diamond interface with a thick interlayer obtained by separately depositing Si. Reprinted with permission from Cheng *et al.*, ACS Appl. Mater. Interfaces **12**, 8376 (2020). Copyright 2020 American Chemical Society.[86] (d) The image of the GaN/diamond heterointerface after direct SAB and 1000 °C annealing. Reprinted with permission from Liang *et al.*, Adv. Mater. **33**, 2104564 (2021). Copyright 2021 Wiley-Blackwell.[89] (e) The image of 1000 °C-annealed GaN/diamond interface with a ~12 nm SiC layer to reduce the roughness of the diamond surface. Reprinted with permission from Kobayashi *et al.*, Funct. Diamond **2**, 142 (2022). Copyright 2022 Taylor & Francis.[104] (f) The image of the GaN/diamond interface with ~1-nm Si interlayer. Reprinted with permission from Matsumae *et al.*, Scr. Mater. **215**, 114725 (2022). Copyright 2022 Elsevier Ltd.[105]

shown in Fig. 17(c). Liang *et al.* achieved room-temperature bonding of Si/diamond interfaces via SAB, as depicted in Fig. 17(d).[112] This work also investigated the effect of annealing. After 1000 °C annealing, the amorphous interlayer recrystallizes, and forms SiC layer. In another similar study, Liang *et al.* fabricated a FET based on a SAB bonded Si/diamond structure.[116] After a 1000 °C-fabrication process, there is no abnormality in the electrical performance of the FET. Together with R. Kagawa *et al.*,[95] these results highlight that the electrical performance of a SAB-bonded interface is qualified for device fabrication. Additionally, Mu *et al.* realized room-temperature bonding of GaN/Si interfaces via SAB.[113] The GaN thin layers bonded to Si substrates at room temperature has sufficient bonding strength, feasible for subsequent device fabrication.[117,118] Though a 5-nm amorphous interlayer occurred, as shown in Fig. 17(e), its thickness may be further reduced by post-annealing.

Ryo Takigawa *et al.* directly bonded a $LiNbO_3$ wafer with SiC without interlayer deposition, as depicted in Fig. 17(f), resulting in an amorphous interlayer thickness less than 5 nm.[114] The room temperature bonding overcomes challenges posed by large CTE differences between SiC and $LiNbO_3$, offering a potential solution to thermal issues in $LiNbO_3$-based devices. AlN was also bonded to a Si wafer by Matsumae *et al.* using SAB.[115] Different bonding conditions were tested, including direct bonding, Si adhesion layer bonding, and Au/Ti adhesion layer bonding, as shown in Fig. 17(g). The measurement of bonding strength under different conditions reveals that the direct bonded interface (0.93 J m^{-2}) exhibits weaker bonding strength compared to interfaces with adhesion layers (>2.5 J m^{-2}). This underscores the importance of interlayers to achieve sufficiently strong bonding, despite the potential hindrance they may pose to heat dissipation across the interface. In a similar work, Xu *et al.* achieved a directly bonded β-Ga_2O_3/SiC interface, demonstrating an average bonding energy of 2.31 J m^{-2}. However, observation of Ga and Si diffusion near the interface due to the annealing process suggests the need for further study.[119]

B. Smart-cut technique

A sufficiently thin device layer on a substrate is crucial for effective thermal management, offering low thermal resistance between the junction and the substrate. This method can be particularly beneficial for materials like β-Ga_2O_3, which possesses relatively low thermal conductivity. The self-heating effect in β-Ga_2O_3 devices poses a significant limitation in device performance. The integration of a nanoscale

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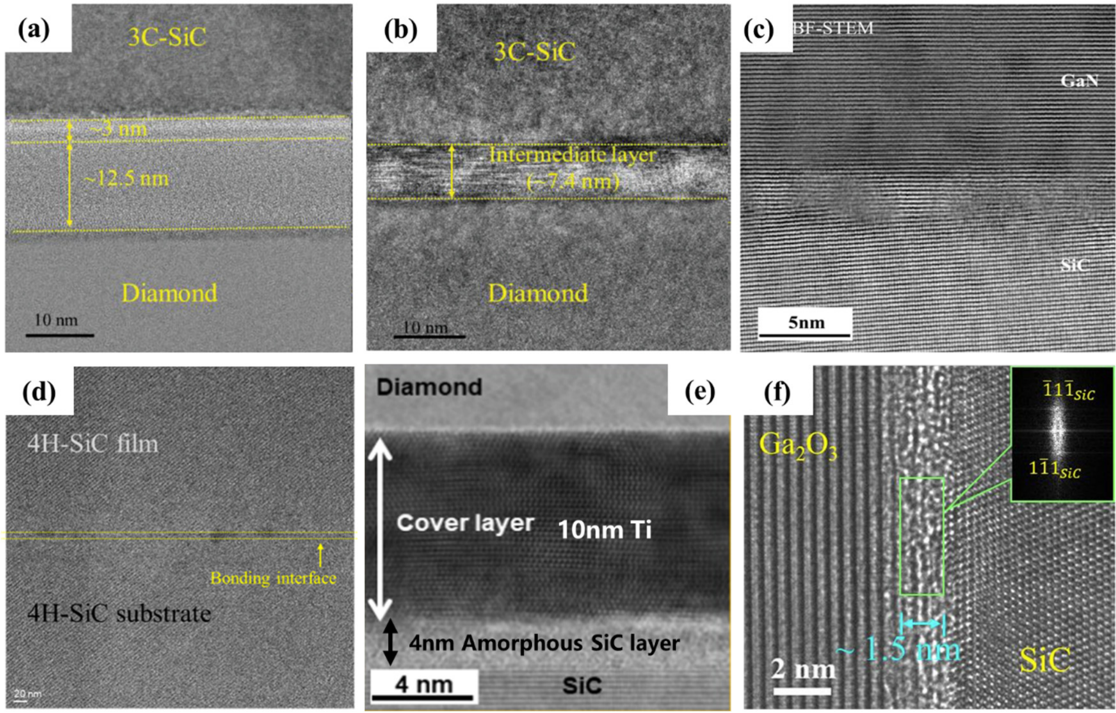

FIG. 15. SAB bonding of some (ultra)wide bandgap semiconductors interfaces. (a) The image of the as-bonded 3C-SiC/diamond interface before annealing. (b) The image of the 3C-SiC/diamond interface after 1100 °C annealing. Reprinted with permission from Kagawa *et al.*, Small **20**, 2305574 (2023). Copyright 2023 Wiley-VCH Verlag.[95] (c) The image of GaN/SiC interface after annealed at 1273 K, with a crystallized interlayer. Reprinted with permission from Mu *et al.*, ACS Appl. Mater. Interfaces **11**, 33428 (2019). Copyright 2019 American Chemical Society.[85] (d) The image of the SiC/SiC interface. Reprinted with permission from Ma *et al.*, ACS Appl. Mater. Interfaces. Copyright 2024 American Chemical Society.[106] (e) The image of a SiC/diamond interface with a 10-nm-thick Ti layer deposited on the diamond surface in advance for protection. Reprinted with permission from Minoura *et al.*, Jpn. J. Appl. Phys., Part 1 **59**, SGGD03 (2020). Copyright 2020 Japan Society of Applied Physics.[107] (f) The image of the 3C-SiC/β-Ga_2O_3 interface after 1100 °C annealing. Reprinted with permission from Liang *et al.*, arXiv:2209.05669 (2022). Copyright 2022 Author(s) under a CC BY 4.0 license.[108]

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monocrystalline thin layer of β-Ga_2O_3 onto a 4H-SiC substrate can be achieved through the smart-cut technique, outlined in Fig. 18(a).[120,121] First, H ions are implanted into the β-Ga_2O_3 wafer, forming a H-rich layer underneath the surface. The wafer is then bonded onto a Si or SiC substrate using SAB. Subsequent annealing leads to the formation and growth of hydrogen gas bubbles at the H-rich layer, resulting in blistering,[122–125] and subsequently, exfoliation of the thin film bonded to the substrate. After polishing the β-Ga_2O_3 thin film and the substrate, the remaining β-Ga_2O_3 can be recycled for further use or fabrication.

Cheng *et al.* conducted bonding of β-Ga_2O_3 thin films on 4H-SiC substrate through smart-cut, involving an Al_2O_3 interlayer deposition via atomic layer deposition (ALD).[24] The transferred β-Ga_2O_3 thin film on 4H-SiC exhibited excellent bonding quality, with a uniformly bonded interface. STEM imaging of the bonded interface after 800 °C annealing in N_2 revealed a slight decrease in the thicknesses of the ALD Al_2O_3 interlayer and amorphous SiC layer, alongside improved crystalline quality of the Al_2O_3 interlayer. Additionally, the annealing process relieved stress originating from ion implantation, thereby reducing phonon scattering and enhancing thermal conductivity. However, Ga diffusion due to the annealing process, alongside potential phonon scattering caused by alloy structure, may affect thermal transport across the interface. Xu *et al.* conducted mapping of thickness across the entire bonding wafer, showing uniform thickness of the bonded β-Ga_2O_3 thin film.[121,126] The normalized x-ray diffractometer rocking curves (XRCs) of its (-201) plane after and before a 900 °C annealing in O_2 for 60 min is shown in Fig. 18(f). The small full width at half maximum of the annealed XRCs indicates that the annealing process can effectively improve the crystal quality of the as-bonded thin film and recover the damage of ions implantation.

Both the β-Ga_2O_3/Al_2O_3 interface and Al_2O_3/SiC interface become amorphous after the bonding, but the amorphous layer at the β-Ga_2O_3/Al_2O_3 interface disappear after the annealing, which is shown in Fig. 18(g). Subsequent experiments demonstrated a significant decrease in device temperature based on such thin film, indicating the practicality of this technique in actual device fabrication. Both studies showcased excellent thermal properties of the β-Ga_2O_3/SiC interface, particularly after annealing, with TBCs reaching as high as 100 and 133 MW m^{-2} K^{-1}, respectively.[24,126] Xu *et al.* bonded β-Ga_2O_3 thin films onto Si or SiC substrates through smart-cut to study the effects of interlayer and post-annealing processes.[127] These findings suggested that the Al_2O_3 interlayer may help prevent element diffusion, resulting in high-quality β-Ga_2O_3 thin films. Additionally, post-annealing processes were proven to recrystallize the interface structure and strengthen bonding strength.

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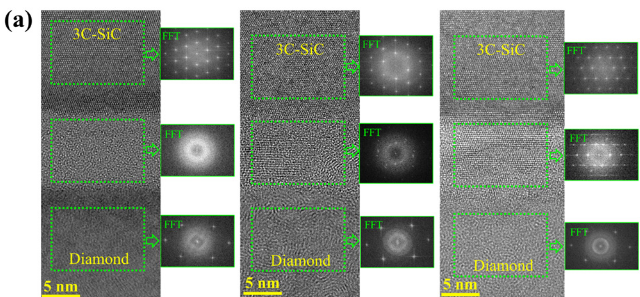

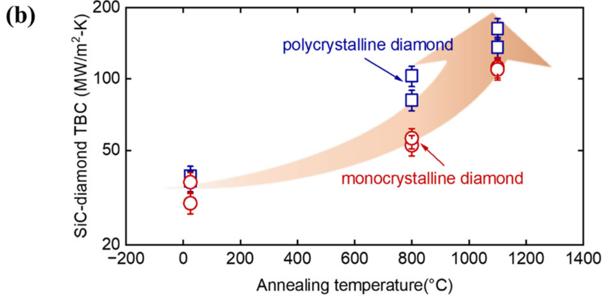

FIG. 16. Bonded 3C-SiC/diamond interfaces with post-annealing process. (a) The TEM images and fast Fourier transform (FFT) images of the as-bonded, 800 °C-annealed, and 1100 °C-annealed interfaces. (b) The TBC increases with annealing temperate. Reprinted with permission from Cheng *et al.*, Adv. Electron. Mater. **2024**, 2400387. Copyright 2024 John Wiley and Sons.[110]

In addition to SAB, another room-temperature bonding method, hydrophilic bonding, can be utilized for bonding two wafers during the smart-cut process. The details and applications of hydrophilic bonding will be discussed in Sec. III C. Shen *et al.* achieved smart-cut through hydrophilic bonding, as depicted in Fig. 19(a).[128] However, to ensure sufficient bonding capable of withstanding high-temperature processes during thin film exfoliation, a thick adhesion layer of Al_2O_3 was intentionally deposited on the surfaces of both wafers. As shown in Fig. 19(b), a ~30 nm thick layer of Al_2O_3 introduces additional thermal resistance that requires further optimization. Xu *et al.* accomplished direct bonding of smart-cut β-Ga_2O_3 on 4H-SiC by hydrophilic bonding.[129] In this study, no intentional interlayer was introduced, resulting in a thin amorphous interlayer, as illustrated in Fig. 19(c). Although further study on the thermal properties of these interfaces is needed, it is anticipated that interfaces with thin interlayers may exhibit high TBCs.

The transfer and bonding of a GaN layer onto a substrate by smart-cut has also been extensively studied.[133–135] Chung *et al.* bonded a GaN thin film onto sapphire using the smart-cut technique, followed by dry etching to remove the damage layer induced by H ions implantation.[136] A layer of MOCVD-GaN was epitaxially grown on the top of the GaN thin films after the bonding. The TEM images of the GaN without dry etching and the dry-etched GaN are shown in Figs. 20(a) and 20(d). The dry etching process effectively removed the damaged layer and result in high-quality GaN.

Shi *et al.* bonded a thin film of GaN to a SiO_2/Si substrate, as depicted in Fig. 20(b).[131] Meanwhile, the GaN near the interface is shown to have high quality, as shown in the area electron diffraction (SAED) pattern in the inset. The image of the bonded GaN-on-Si wafer is shown in Fig. 20(c). Liu *et al.* achieved direct bonding of a GaN thin film onto a Si substrate without any intentionally deposited interlayer.[132] The TEM image of the bonded interface is shown in Fig. 20(e), where the GaN/Si interface is strongly bonded and only has a thin interlayer. Fig. 20(f) shows a thin layer of uniform ReS_2 grown on the top of GaN thin film for further device fabrication.

Qin *et al.* bonded a thin layer of AlN onto a Si substrate by the smart-cut method. Figure 21 shows the evaluation of the bubbles during the ion implantation and blistering process.[137] Figure 21(a) illustrates the evaluation of blister cracks over time, with bubbles enlarging and increasing in quantity, ultimately resulting in weak bonding near the ion-rich layer. Figure 21(b) shows the optical microscopy (OM) image of the bonded AlN surface, where no voids or cracks are observed. Figure 21(c) shows the TEM image of the AlN/SiO_2 interface, similar to the aforementioned GaN/Si structure. The thick SiO_2 isolator layer is from the thermal oxide layer on the Si substrate.

Due to the high cost of high-quality SiC, the smart-cut technique is used to fabricate high-quality SiC thin films bonded on low-cost substrates. The high-quality SiC thin films can be used for further device fabrication similar to those on the bulk high-quality SiC substrate.[139] Yi *et al.* bonded a 4H-SiC thin film onto a SiO_2/Si substrate by smart-cut technique.[138] Figure 22(a) shows the bonded 4H-SiC thin film on SiO_2/Si wafer. No obvious voids or cracks are observed, indicating a uniform bonding. Figure 22(b) shows the TEM image of the SiC/SiO_2/Si interface. Sharp interfaces can be observed and no defects or damage were found in the 4H-SiC layer.

Most smart-cut semiconductor heterostructures mentioned above lack experimental measurements of their thermal properties, such as thermal conductivity and TBC between the films and substrates. Therefore, this area warrants further investigation. For the structures involving thick SiO_2 layers,[131,137,138] such thick layer of low thermal conductivity material is expected to seriously hinder thermal transport between the device layer and the substrate. Efforts should be made to reduce the thickness of the isolator layer while minimizing its impact on device performance.

C. Hydrophilic bonding

In addition to SAB, hydrophilic bonding emerges as another crucial technique for integrating (ultra)wide bandgap semiconductors, potentially offering high TBC due to the presence of thin interfacial layers. Similar to SAB, the surfaces of the two to-be-bonded wafers must undergo polishing, achieving a surface roughness below 0.5 nm (RMS). Subsequently, the diamond substrate undergoes a cleaning process using H_2SO_4/H_2O_2 and NH_3/H_2O_2 solutions, while the Si substrate is treated by oxygen plasma in reactive ion etching (RIE). Following these preparations, the two wafers are pressed together at atmospheric air and annealed at 250 °C, as depicted in Fig. 23(a).[140] Cross-sectional TEM images of bonded interfaces through the hydrophilic bonding technique, such as Si/diamond, GaN/Si, β-Ga_2O_3/diamond, GaN/diamond, β-Ga_2O_3/SiC, and SiO_2/diamond interfaces, are presented in Figs. 23(b)–23(g). In contrast to the aforementioned SAB techniques, which require a vacuum bonding environment, hydrophilic bonding circumvents such extreme processes and conditions, minimizing damage to the crystal structure. Figure 23(b) shows an interface between diamond and Si attained by hydrophilic bonding.[141] This structure did not undergo Ar ions activation. As a result, a thin interlayer of 2.5 nm SiO_2 appeared, which is thinner compared to the

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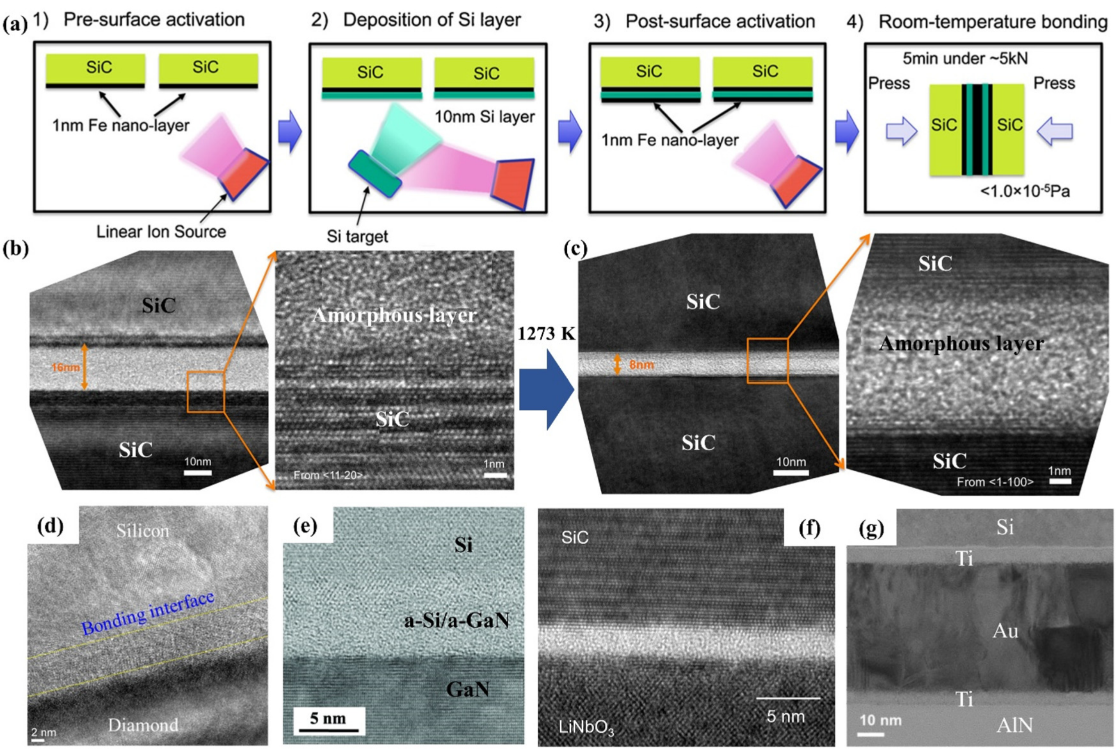

FIG. 17. Other (ultra)wide bandgap semiconductor interfaces bonded by SAB. (a) A modified SAB method which deposits Si interlayer by Ar ion sputtering. (b) The image of the as-bonded SiC/SiC interface with a thick amorphous interlayer. (c) The image of the SiC/SiC interface after annealing at 1273 K, which indicates the decrease in the amorphous interlayer's thickness. Reprinted with permission from Suga *et al.*, Jpn. J. Appl. Phys., Part 1 **54**, 030214 (2015). Copyright 2015 IOP Publishing.[111] (d) The image of an 800 °C-annealed direct bonding Si/diamond interface. Reprinted with permission from Liang *et al.*, Diamond Relat. Mater. **93**, 187 (2019). Copyright 2019 Elsevier BV.[112] (e) The image of directly bonded Si/GaN interface with amorphous Si and GaN interlayer. Reprinted with permission from Mu *et al.*, Appl. Surf. Sci. **416**, 1007 (2017). Copyright 2017 Elsevier.[113] (f) The image of a SiC/$LiNbO_3$ interface fabricated by SAB. Reprinted with permission from Takigawa *et al.*, Scr. Mater. **174**, 58–61 (2020). Copyright 2020 Elsevier.[114] (g) The image of a AlN/Si interfaces obtained by SAB with a Ti/Au/Ti interlayer. Reprinted with permission from Matsumae *et al.*, Ceram. Int. **46**, 25956–25963 (2020). Copyright 2020 Elsevier.[115]

as-bonded SAB interlayer mentioned above. Several studies have been carried out on the room-temperature hydrophilic bonding of diamond/Si interface.[142–145] Most of them show high quality bonding of crystals with a thin interlayer, which highlights the feasibility of hydrophilic bonding. Other pairs of interfaces bonded by hydrophilic bonding are GaN/Si in Fig. 23(c), Ga_2O_3/diamond in Fig. 23(d), GaN/diamond in Fig. 23(e), Ga_2O_3/diamond in Fig. 23(f), and SiO_2/diamond in Fig. 23(g).[140,141,146–150] Thin interlayers and high-crystal quality are found among these structures. Although thermal characterizations are still lacking, these interfaces are expected to have high TBC due to the well-structured interface. However, a drawback of the hydrophilic bonding technique is the instability of bonded interfaces at high temperatures. For real-world applications, devices need to be fabricated first and then bonded with other materials. The uniformity of bonded interfaces over a large area also requires further investigation.

D. Plasma bonding

Plasma bonding is another robust bonding method capable of forming strong bonds.[154] The mechanism of plasma bonding shares similarities with SAB. SAB employs surface activation achieved through Ar ion implantation, while plasma bonding utilizes Ar, O_2, or N_2 plasma.[155] Jian *et al.* conducted plasma bonding of a β-Ga_2O_3/GaN interface.[151] As illustrated in Fig. 24(a), atomically smooth surfaces of β-Ga_2O_3 and GaN were activated by acid and atmospheric plasma, followed by bonding the two wafers under pressure without depositing an interlayer. The TEM image of the as-bonded interface [Fig. 24(b)] reveals no voids. However, an amorphous interlayer appeared when the structure underwent 900 °C annealing in N_2, necessitating further investigation. Matsumae *et al.* explored the effect of O_2 and N_2 used during surface activation in plasma bonding of GaN and Si.[152] Different activation conditions were tested, as depicted in Fig. 24(d). The results indicated that, for bonding of GaN and Si, single use of O_2 or N_2 failed to form sufficiently strong bonds; only sequential plasma activation led to strong adhesion, as evidenced by the TEM image of the interface [Fig. 24(e)]. Another study focused on the effect of plasma components was conducted by Kang *et al.*[153] Figures 24(f) and 24(g) are the TEM images of two interfaces bonded in N_2 plasma and O_2 plasma after annealing at 150 °C. It shows that only O_2 plasma can form a uniform interface without voids and cracks. However more bubbles area would form in the interface in O_2 atmosphere, as shown in Fig. 24(h).

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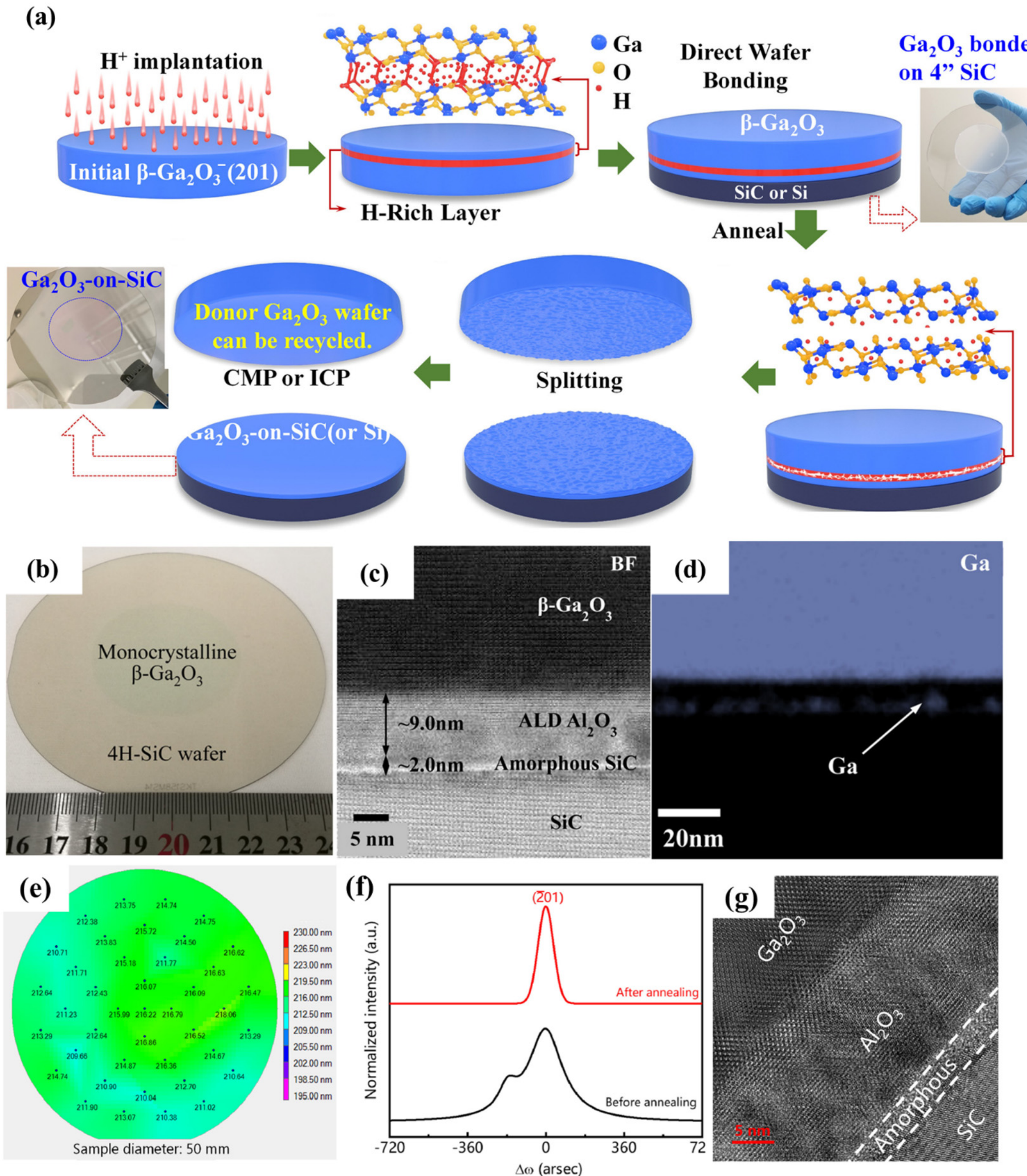

FIG. 18. The β-Ga_2O_3 thin films on Si or SiC substrate transferred and bonded by smart-cut technique. (a) The procedures of smart-cut, including ion implantation, SAB, exfoliation, and polishing. Reprinted with permission from Li *et al.*, Fundam. Res. (published online) (2023). Copyright 2023 Elsevier.[121] (b) A thin film of β-Ga_2O_3 transferred on a 4 in. 4H-SiC wafer. (c) The STEM image of the β-Ga_2O_3-SiC interface after annealing. (d) The Ga distribution near the bonded interface after annealing obtained by EELS, indicating the diffusion of Ga. Reprinted with permission from Cheng *et al.*, ACS Appl. Mater. Interfaces **12**, 44943 (2020). Copyright 2020 American Chemical Society.[24] (e) The thickness variation of a 2 in. β-Ga_2O_3 thin film. (f) The XRCs of the β-Ga_2O_3 thin film after and before a 450 °C annealing process. (g) The image of the β-Ga_2O_3/Al_2O_3/SiC interface produced by smart-cut after 450 °C annealing. Reprinted with permission from Li *et al.*, Fundam. Res. (published online) (2023). Copyright 2023 Elsevier.[121]

Kang *et al.* fabricated a GaN/BAs interface by plasma bonding with an Al_2O_3 interlayer deposited by ALD. SEM and TEM images of the bonded interface after a 773 K annealing showed a 2-nm-thick interlayer, as illustrated in Figs. 25(a) and 25(b).[156] The TBC of this interface was measured to be 250 MW m^{-2} K^{-1}, much higher than the TBC of the diamond/GaN interface, attributed to the better matching of the phonon dispersion relations of BAs and GaN.[156] Nieminen *et al.* bonded an AlN wafer onto a Si wafer through plasma bonding.[157] A 10-nm oxide multilayer appeared at the interface, as shown in Fig. 25(c). The TBC of this interface was measured to be 105 MW m^{-2} K^{-1}, even larger than the deposited AlN/Si interface in the same study. The authors attributed this high TBC to the high quality of the adhesive interlayer.

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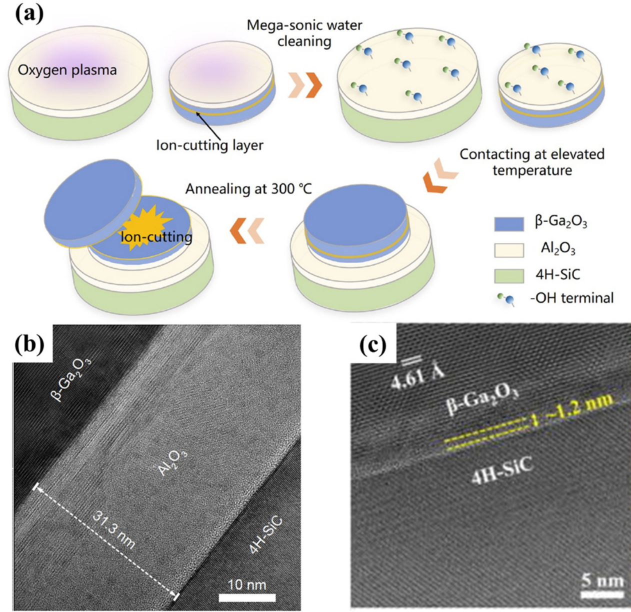

FIG. 19. Smart-cut achieved by hydrophilic bonding process. (a) The procedure. (b) The image of the β-Ga_2O_3/4H-SiC interface with a thick interlayer. Reprinted with permission from Shen *et al.*, Sci. China Mater. **66**, 756–763 (2023). Copyright 2023 Springer Nature.[128] (c) The TEM image of another hydrophilic bonding smart-cut β-Ga_2O_3/4H-SiC interface without intentionally deposited interlayer. Reprinted with permission from Xu *et al.*, Appl. Phys. Lett. **124**, 112102 (2024). Copyright 2024 AIP Publishing LLC.[28]

E. Other bonding methods

Jian *et al.* demonstrated the bonding of a β-Ga_2O_3/GaN interface through the diffusion of a ZnO layer deposited by ALD. The procedure is depicted in Fig. 26(a). After high temperature and pressure, ZnO diffused into the β-Ga_2O_3 layer, as shown in Fig. 26(b). The adhesive ZnO layer helped fully bond the interface. Additionally, Zhong *et al.* performed eutectic bonding of Si and diamond, as shown in Fig. 26(c).[93] Multilayers of Ti/Cu/Ti/Au and Ti/Au were deposited on diamond and Si. Two wafers were pre-bonded at room temperature through the diffusion of Au atoms at the interface. The TEM image of the pre-bonded interface is shown in Fig. 26(d). Subsequently, Cu-Au atoms began interdiffusion during low temperature annealing, eventually forming a firm interface. The TEM image of the final interface is depicted in Fig. 26(e), showing multiple boundaries and interfaces. The TBC of this diamond/Si interface was measured to be 103 MW m^{-2} K^{-1}, a high TBC among diamond-related interfaces, while the details of thermal measurement process is lacking in the paper. This TBC value needs to be double checked since the interfacial layer is as thick as 250 nm (cannot be treated as an interface in the thermal model) and composed of mixed nanocrystalline metallic alloy.

Delmas *et al.* reported a bonding method utilizing both eutectic bonding and Ar plasma activation, achieving room-temperature bonding of the GaN/diamond interface under low-vacuum environment without the need for high vacuum processes in traditional SAB.[159] The bonding process is depicted in Fig. 27(a). Before Ar plasma activation, a layer of Ti/Au was deposited on the surfaces of both wafers, followed by compression. The TEM image of the interface is presented in Fig. 27(b), where some voids at the interface appeared. The map of the

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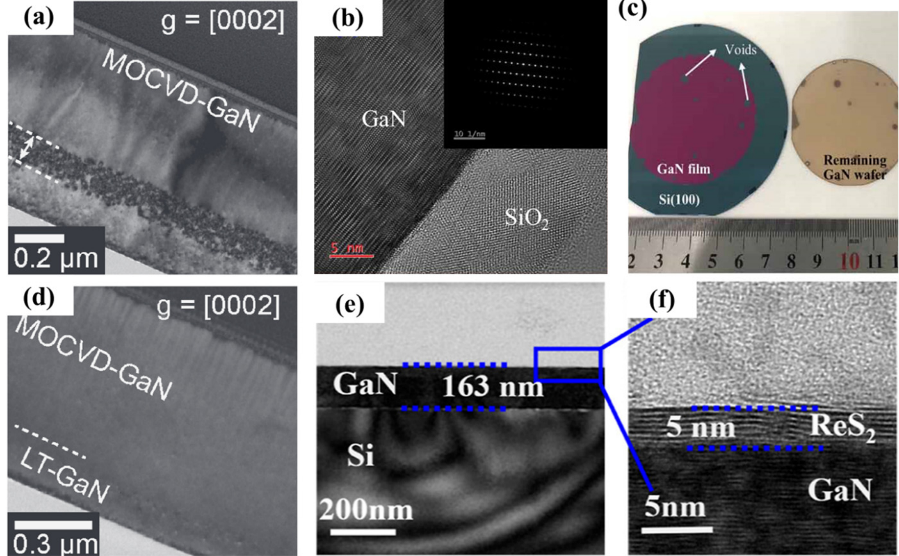

FIG. 20. Smart-cut of GaN thin films. (a) The image of the MOCVD-GaN grown on the layer-transferred GaN surface.[29] (b) The image of the GaN/SiO_2 interface after 800 °C annealing. (c) The picture of a GaN-on-Si wafer and the remaining GaN for recycle. Reprinted with permission from Shi *et al.*, Semicond. Sci. Technol. **35**, 125004 (2020). Copyright 2020 IOP Publishing Ltd.[131] (d) The TEM image of the MOCVD-GaN grown on the dry-etched layer-transferred GaN surface. Reprinted with permission from Chung *et al.*, Appl. Phys. Express **6**, 111005 (2013). Copyright 2013 IOP Publishing, Ltd.[130] (e) The TEM image of the interface of a GaN thin film directly bonded to the Si substrate without interlayer (f) The TEM image of a ReS_2 layer grown on the top of the transferred GaN thin film. Reprinted with permission from Liu *et al.*, ACS Omega **8**457 – 463 (2023). Copyright 2023 American Chemical Society.[132]

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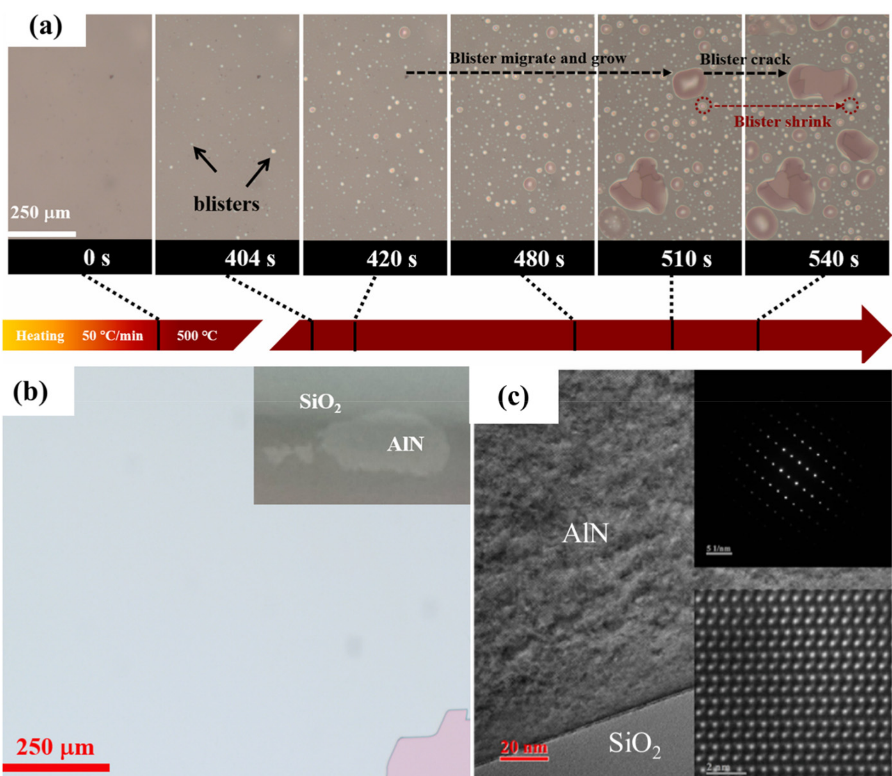

FIG. 21. AlN/Si heterostructure fabricated by smart-cut (a) The evaluation of the blister cracks of a bonded AlN/Si interface over time. (b) The optical microscopy image of the surface of the as-transferred AlN/Si (the inset shows a picture of the surface). (c) The TEM image of a AlN/Si interface after post-annealing process with a thick SiO_2 interlayer. Reprinted with permission from Qin *et al.*, Mater. Sci. Semicond. Process. **176**, 108346 (2024). Copyright 2024 Elsevier Ltd.[137]

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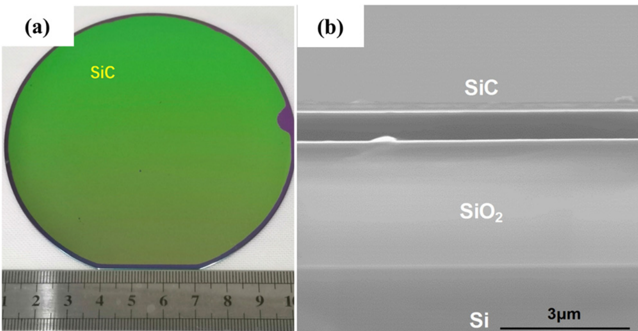

FIG. 22. SiC/Si heterostructures fabricated by smart-cut. (a) 4H-SiC on insulator (4H-SICOI) wafer fabricated by smart-cut. (b) The TEM image of 1100 °C-annealed SiC-SiO_2 interface. Reprinted with permission from Yi *et al.*, Opt. Mater. **107**, 109990 (2020). Copyright 2020 Elsevier.[138]

phase shift at different frequency-domain thermoreflectance (FDTR) frequencies is displayed in Fig. 27(c). As the frequency decreases, the thermal penetration depth increases, so the TBC of the interface is clearly detected. The mapping region contained the well-bonded region (the red box), the unbonded region (the black box), and a not fully bonded region (the blue box).

Utilizing the fusion bonding method, Song *et al.* fabricated a β-Ga_2O_3/4H-SiC interface, as shown in Fig. 28(a).[160] The bonded wafer is depicted in Fig. 28(b), indicating high bonding quality as no significant cracks or unbonded areas are visible. The TEM image of the interface is shown in Fig. 28(c), revealing an obscure interface formed during the fusion process, with an interlayer of SiO_x. Thermal characterization indicated a TBC of $\sim$22 MW m^{-2} K^{-1}, likely influenced by the thick interlayer of SiN and SiO_x.

F. Summarization of TBC values

Here, we summarize the TBCs of different (ultra)wide bandgap semiconductor interfaces fabricated by different methods, including SAB, smart-cut, plasma bonding, fusion bonding, eutectic bonding, hydrophobic bonding, hydrophilic bonding, van der Waals bonding, CVD, MOCVD, hot-filament CVD (HFCVD), microwave plasma CVD (MWCVD or MPCVD), low-pressure MOCVD (LP-MOCVD), and so on (Table II).

IV. CHARACTERIZATION, ENHANCEMENT, AND UNDERSTANDING OF TBC

Building upon Sec. III, Sec. IV delves into pivotal research concerning the TBC of heterostructures. This section is subdivided into three key components: characterizations, predominantly encompassing the diverse methodologies employed for TBC measurement; enhancement strategies, comprising both experimental and theoretical approaches; and finally, the fundamental comprehension of TBC, particularly concerning the interfacial phonon mode.

A. Thermal characterization of TBC

Thermal characterization techniques are indispensable the comprehension of thermal conduction in (ultra)wide bandgap

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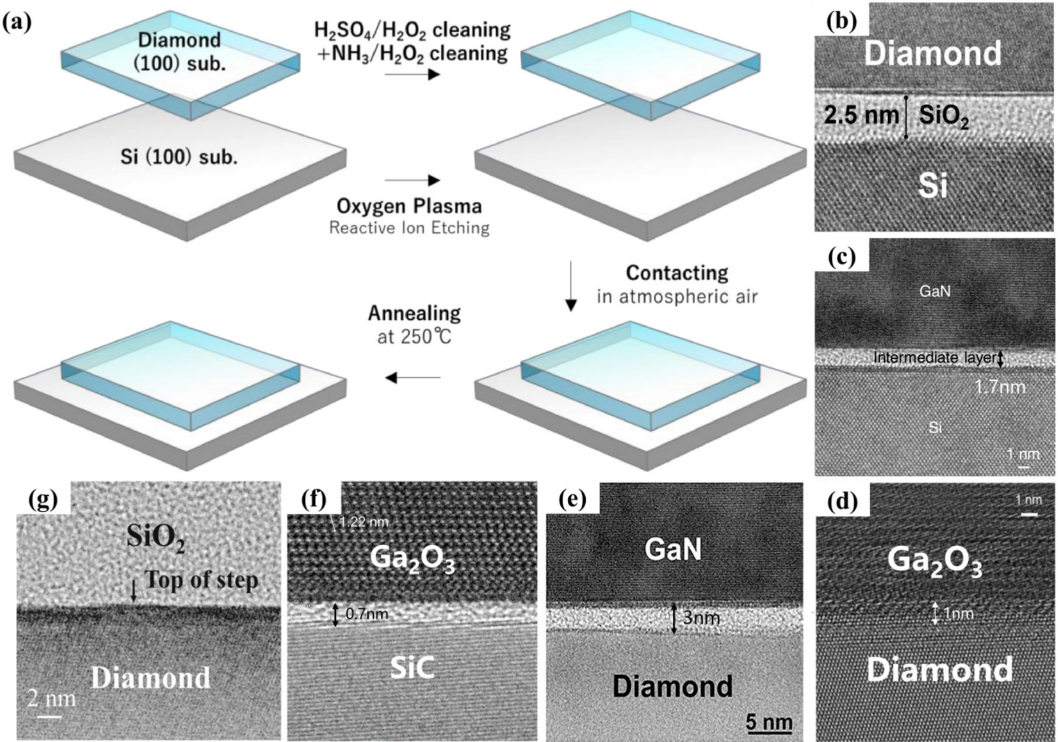

FIG. 23. Hydrophilic bonding. (a) The main processes of hydrophilic bonding include cleaning and oxygen plasma treatment of the surfaces, keeping the two surfaces in contact, and annealing. Reprinted with permission from Matsumae *et al.*, Scr. Mater. **191**, 52 (2021). Copyright 2021 Elsevier Ltd.[140] (b)–(g) The TEM images of different interfaces obtained by hydrophilic bonding. (b) The interface of Si-diamond with SiO_2 interlayer formed during the process. Reprinted with permission from Fukumoto *et al.*, Appl. Phys. Lett. **117**, 201601 (2020). Copyright 2020 AIP Publishing LLC.[141] (c) The GaN/Si interface with ∼1.7 nm-thick amorphous intermediate layer. Reprinted with permission from Fukumoto *et al.*, Jpn. J. Appl. Phys., Part 1 **61**, SF1005 (2022). Copyright 2022 Japan Society of Applied Physics.[146] (d) The β-Ga_2O_3/diamond interface. Reprinted with permission from Matsumae *et al.*, Appl. Phys. Lett. **116**, 141602 (2020). Copyright 2020 AIP Publishing LLC.[147] (e) The GaN–diamond interface. Reprinted with permission from Matsumae *et al.*, ACS Appl. Nano Mater. **6**, 14076 (2023). Copyright 2023 American Chemical Society.[148] (f) The β-Ga_2O_3/SiC interface. Reprinted with permission from Matsumae *et al.*, J. Appl. Phys. **130**, 085303 (2021). Copyright 2021 AIP Publishing LLC.[149] (g) The interface between diamond and SiO_2-Si substrate with deformed SiO_2 interlayer filling the nanogaps. Reprinted with permission from Matsumae *et al.*, Jpn. J. Appl. Phys., Part 1 **59**, SBBA01 (2020). Copyright 2020 Japan Society of Applied Physics.[150]

semiconductor heterostructures. Evaluating the thermal properties of materials and interfaces, particularly through the measurements of TBC, serves as the cornerstone for optimizing growth and integration processes. Furthermore, thermal characterizations facilitate the assessment of device thermal performance, as discussed in Sec. III. In this segment, we provide a brief overview of thermal characterization techniques, with a particular focus on TBC measurements.

1. Pump–probe techniques

Pump–probe thermoreflectance techniques, encompassing time-domain thermoreflectance (TDTR),[206,207] frequency-domain thermoreflectance (FDTR),[208,209] and nanosecond transient thermoreflectance (nanosecond-TTR),[210,211] have been extensively employed for spatially resolved characterization of thermal transport properties in multilayer structures.[212] In these techniques, an ac temperature excursion is induced at the sample surface through optical absorption of the intensity-modulated pump laser. The surface temperature excursion is then detected by the intensity changes of the reflected probe laser, relying on the temperature dependence of optical reflectivity. Typically, a ∼80-nm-thick metal thin film is coated on the sample to facilitate optical absorption and temperature detection.

TDTR utilizes an ultra-fast pulsed laser source. This train of laser pulses is then split into the pump and probe beams. The pump beam is modulated to create periodic heating of the sample surface while the probe beam detects the variation of the temperature of the sample surface. The recorded signal is measured as a function of the delay time between the pump laser and the probe laser. The detected region is characterized by the thermal penetration depth, d_p, defined as $d_p = \sqrt{k/C\pi f}$,[36,213] where f is the modulation frequency, C is the volumetric heat capacity of the material, and k is the thermal conductivity.

In FDTR, the ultra-fast laser source is replaced by one or two CW laser sources.[209] The signal is obtained by varying the modulation frequency of the pump beam from a few hundreds of Hz to tens of MHz,[214] in some cases ultra-low modulation frequency is also applied to measure the deeply buried structures.[215] Compared to TDTR, FDTR simplifies the light path and instrumentation. However, because the frequency range is shifted from high to low, the penetration depth in

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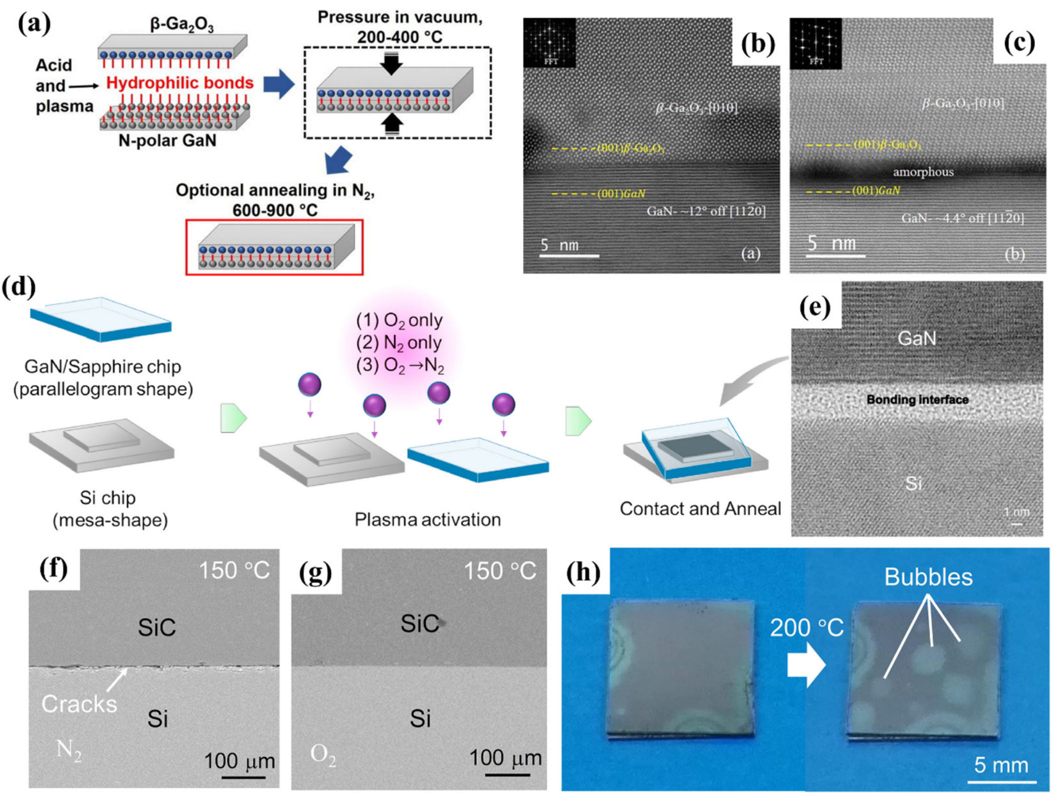

FIG. 24. The plasma bonding. (a) The procedure of plasma bonding, including surface activation, bonding, and post-annealing. (b) The TEM image of the as-bonded β-Ga_2O_3/GaN interface. (c) The TEM image of the β-Ga_2O_3/GaN interface after 900 °C in N_2. Reprinted with permission from Jian *et al.*, Appl. Phys. Lett. **120**, 142101 (2022). Copyright 2022 AIP Publishing LLC.[151] (d) The work flow of the O_2/N_2 plasma activation procedure. (e) The TEM image of the bonded GaN/Si interface. Reprinted with permission from Matsumae *et al.*, J. Alloys Compd. **852**, 156933 (2021). Copyright 2021 Elsevier.[152] (f) The TEM image of SiC/Si interface bonded by N_2 plasma activation. (g) The TEM image of SiC/Si interface bonded by O_2 plasma activation. (h) Pictures of SiC/Si before and after 200 °C annealing. Reprinted with permission from Kang *et al.*, Ceram. Int. **46**, 22718–22726 (2020). Copyright 2020 Elsevier.[153]

FDTR is larger than that in TDTR, resulting in lower spatial resolution and a lower sensitivity to TBC. Moreover, application of FDTR at high frequency is limited by a frequency dependence of measured thermal conductivity.[216] The ability of TBC measurement of FDTR is also limited by the adhesion layer. A layer of Au is deposited on to the sample's surface as a transducer in FDTR and a layer of Ti or Cr is inserted between the Au layer and the substrate as an adhesion layer. The additional thermal resistance introduced by the adhesion layer further lower the sensitivity of TBC.[214,216]

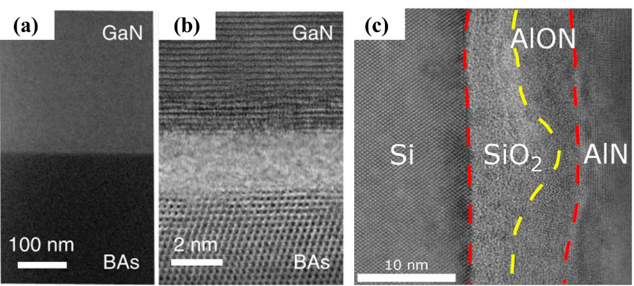

FIG. 25. Integration by plasma bonding. (a) Cross-sectional image of a GaN/BAs interface (b) Cross-sectional TEM of a GaN/BAs interface with an Al_2O_3 interlayer. Reprinted with permission from Kang *et al.*, Nat. Electron. **4**, 416–423 (2021). Copyright 2021 Springer Nature.[156] (c) The plasma-bonded AlN/Si interface with a thick interlayer. Reprinted with permission from Nieminen *et al.*, ACS Appl. Electron. Mater. Copyright 2024 American Chemical Society.[157]

TTR is the early version pump–probe technology, originally developed to study electron–phonon coupling in metal films.[217] Nowadays, nanosecond pulsed laser is used to heat the sample surface. Unlike TDTR and FDTR, nanosecond-TTR does not utilize frequency modulation of the heating laser and lock-in detection of the temperature response.[210] Instead, it utilizes the temperature change due to a single pulse heating by the pump beam as a function of time, which is detected by the thermoreflectance signal of a CW laser probe. Due to the generally low thermoreflectance coefficient ($\sim 10^{-4}$ K^{-1}), nanosecond-TTR has a low signal-to-noise ratio (SNR). To address this limitation, multiple pulses are employed to reduce random noise through the averaging of tens of thousands of acquisition periods.[211,218] The averaging of signal can eliminate the random noise but cannot reduce the other noises such as $1/f$ noise in the signal.[217]

The steady-state thermal response of the material under laser heating can also be utilized for thermal characterization. Steady-state

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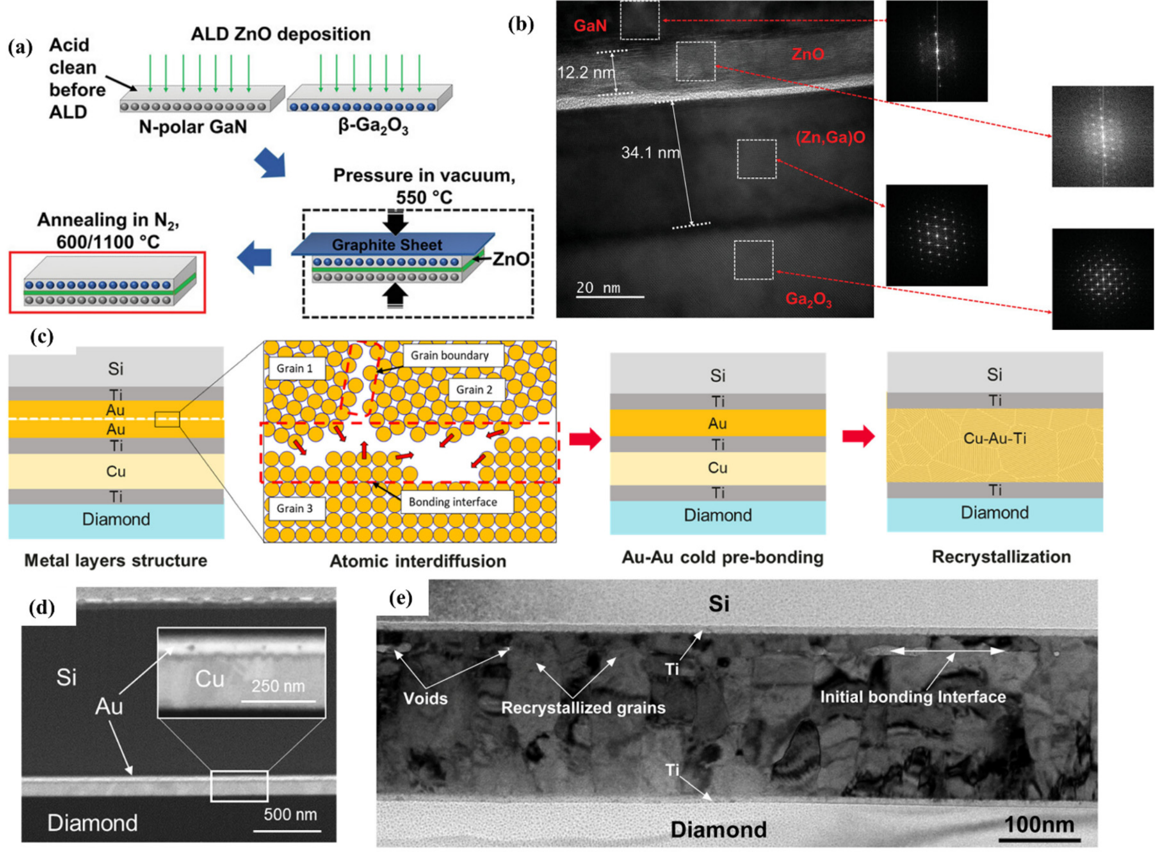

FIG. 26. Interface fabricated by other bonding methods (a) The process of the bonding of β-Ga_2O_3/GaN through the diffusion of a ZnO interlayer. (b) The TEM image of the β-Ga_2O_3/GaN interface. ZnO diffuses into β-Ga_2O_3 layer. Reprinted with permission from Jian *et al.*, Adv. Electron. Mater. **9**, 2300174 (2023). Copyright 2023 John Wiley and Sons.[158] (c) The mechanism of eutectic bonding of a Si/Ti/Au/Cu/diamond structure, including the Au–Au pre-bonding at room temperature and low-temperature Cu–Au–Ti recrystallization. (d) The TEM image of the bonded interface. (e) The TEM image of the interface after recrystallization. Reprinted with permission from Zhong *et al.*, J. Mater. Sci. Technol. **188**, 37–43 (2024). Copyright 2024 Elsevier.[93]

thermoreflectance (SSTR),[219] operating at the low-frequency limit where the temperature response on the sample's surface reaches a steady-state value and the thermal diffusion length, is significantly larger than the laser beam radius. The probing depth is tunable within the range of micrometers to millimeters depending on the laser beam radius.[212] In SSTR, the CW pump laser is intensity-modulated at a sufficiently low frequency. Similar to other thermoreflectance techniques, the surface temperature change is detected by the thermoreflectance signal of the probe laser, but the thermoreflectance coefficient needs to be calibrated in SSTR because the magnitude of the temperature change as a function of the power of a CW pump laser is used to determine the thermal conductivity of the sample via Fourier's law.

It is important to note that the accuracy of SSTR measurement hinges on the dominant role of the thermal resistance of interest in the overall thermal resistance in the probed volume, as dictated by the radius of pump/probe laser beams. If the TBC of the interface between the thin film and substrate is exceptionally low (i.e., $5\mathrm{MW/m_2{-}K}$), the measurement of the buried substrate becomes challenging, but the measurement of TBC becomes feasible. If the TBC of the buried interfaces is high, the sensitivity to the TBC is negligible and thus the measurement of TBC becomes challenging.

In addition to the thermoreflectance signal, other probing signals can be leveraged to detect the ac temperature Immersion thermo-optic phase spectroscopy (I-TOPS) has been recently developed for fast measurement of the thermal conductance of thin films and interfaces.[220] With the sample immersed in a transparent liquid, the deflection of the probe beam in the liquid, resulting from the thermally induced gradient of refractive index, serves as the thermometer. Alternatively, a transparent monomer (e.g., PDMS) can be cured on the sample in place of the liquid. Similar to SSTR, the pump beam is intensity-modulated at a sufficiently low frequency, allowing the heat conduction in the sample to approach steady state. The magnitude of probe beam deflection is then used to extract the thermal conductance of the sample. The probing depth scales with the pump/probe beam radius and thus be tunable in the similar range of SSTR. Compared to methods based on thermoreflectance, I-TOPS has a much larger SNR, which enables orders of magnitude faster measurements. For all other

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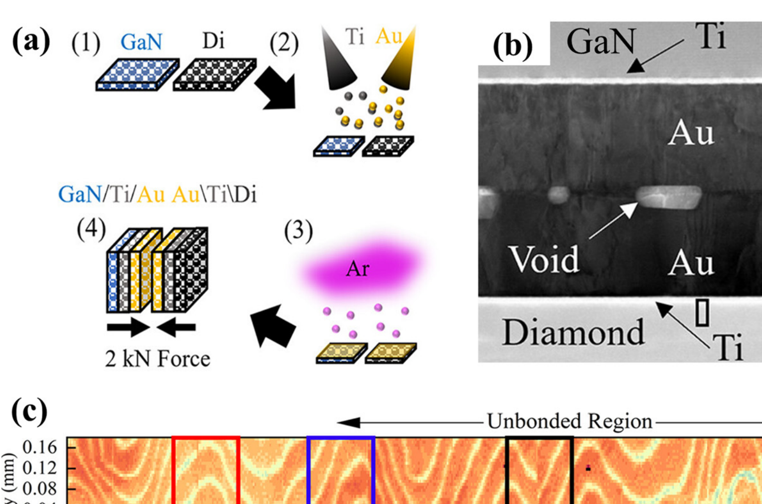

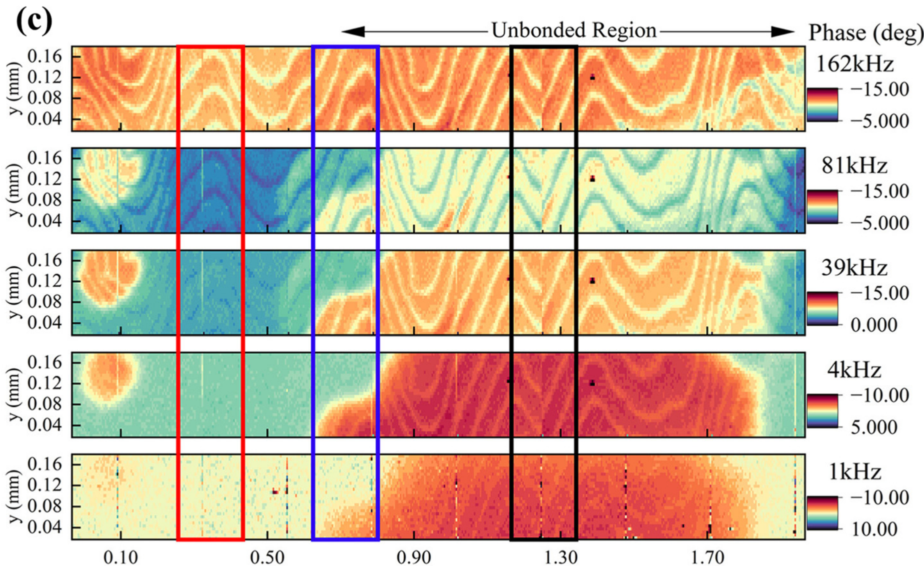

FIG. 27. A combination of eutectic bonding and plasma bonding. (a) The process of the bonding method, including the deposition of metal layer, Ar plasma activation, and compression. (b) The TEM image of the bonded interface. (c) FDTR mapping under different modulation frequencies. Reprinted with permission from Delmas *et al.*, ACS Appl. Mater. Interfaces **16**, 11003 – 11012 (2024). Copyright 2024 American Chemical society.[159]

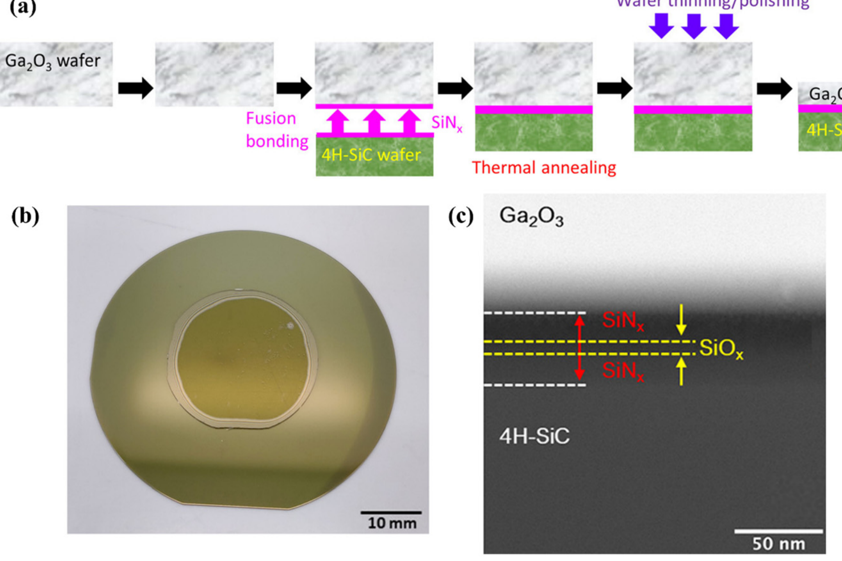

FIG. 28. The fusion bonding of β-Ga_2O_3/4H-SiC interface. (a) The bonding process. (b) The picture of the bonded wafer. (c) The TEM image of the bonded interface. Reprinted with permission from Song *et al.*, ACS Appl. Mater. Interfaces **13**, 14 (2021). Copyright 2021 America Chemical Society.[160]

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TABLE II. Summary of TBCs of different (U)WBG semiconductors related interfaces and their corresponding fabrication methods.

Materials	Method	Interlayer	TBC ($MW\ m^{-2}\ K^{-1}$)	References
Si/diamond	Graphoepitaxy	None	64	83
Si/diamond	Graphoepitaxy	105 × 210 nm teeth	80	83
Si/diamond	Graphoepitaxy	47 × 69 nm teeth	105	83
Si/diamond	HFCVD	None	50	161
Si/diamond	CVD	None	50–100	162
Si/diamond	CVD	10 nm a-layer	∼67	163, 164
Si/diamond	CVD	Not mentioned	18	65
Si/diamond	Eutectic bonding	Ti(8 nm)/Cu-Au-Ti(∼200 nm)/Ti(8 nm)	103	93
Si/SiC	CVD	None	620	7
Si/SiC	Hydrophobic bonding	0.2–0.5 nm a-SiO_2	167	166
Si/SiC	Hydrophilic bonding	0.5 nm a-SiO_2	111	166
GaN/diamond	Mixed-size seeding CVD	130 nm cry-AlN	>167	167
GaN/diamond	MOCVD	1 nm Si_3N_4	323	168
GaN/diamond	MOCVD	10 nm Si_3N_4	83	168
GaN/diamond	HFCVD	34 nm SiN_x	40	169
GaN/diamond	MWCVD	100 nm SiN_x	20	169
GaN/diamond	MWCVD	28 nm SiN_x	83	169
GaN/diamond	HFCVD	50 nm SiN_x +50 nm a-layer	24	169
GaN/diamond	HFCVD	50 nm SiN_x +20 nm a-layer	30	169
GaN/diamond	MWCVD	36 nm SiN_x	30	169
GaN/diamond	MWCVD	41 nm SiN_x	36	169
GaN/diamond	MWCVD	None	24	170
GaN/diamond	MWCVD	5 nm AlN	55	170
GaN/diamond	MWCVD	5 nm SiN_x	105	170
GaN/diamond	MWCVD	10 nm c-SiC	33	171
GaN/diamond	MWCVD	Not mentioned	9	171
GaN/diamond	MPCVD	Not mentioned	18	172
GaN/diamond	MPCVD	Not mentioned	28	172
GaN/diamond	MPCVD	70 nm a-layer	12	172
GaN/diamond	MPCVD	35 nm a-layer	38	172
GaN/diamond	CVD	250 nm AlN	63	173
GaN/diamond	MPCVD	none	16	174
GaN/diamond	MPCVD	5 nm a-AlN	63	174
GaN/diamond	MPCVD	5 nm a-SiN	154	174
GaN/diamond	CVD	50 nm dielectric	59	175
GaN/diamond	CVD	90 nm dielectric	24	175
GaN/diamond	CVD	50 nm dielectric	56	176
GaN/diamond	MPCVD	25 nm dielectric	37	177
GaN/diamond	MPCVD	50 nm dielectric	28	177
GaN/diamond	PVD	Ti (5 nm)/AuSn (40 nm)/Ti (5 nm)	13	178
GaN/diamond	MBE	None	>100	179
GaN/diamond	MWCVD	50 nm a-Si_3N_4	11–22	180
GaN/diamond	HFCVD	46 nm SiN_x	19	181
GaN/diamond	MWCVD	18 nm SiN_x	25	182
GaN/diamond	High-temperature bonding	3–42 nm dielectric	28	83
GaN/diamond	High-temperature bonding	38–55 nm dielectric	21	83
GaN/diamond	High-temperature bonding	31 nm SiN	31	184
GaN/diamond	High-temperature bonding	22 nm SiN	51	184
GaN/diamond	High-temperature bonding	22 nm SiN	57	184

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TABLE II. (*Continued.*)

Materials	Method	Interlayer	TBC (MW m^{-2} K^{-1})	References
GaN/diamond	van der Waals bonding	None	5	185
GaN/diamond	SAB	15 nm Si + 3 nm a-layer	32	102
GaN/diamond	SAB + 800 °C annealing	15 nm Si + 3 nm a-layer	71	102
GaN/diamond	SAB	22 nm Si + 3 nm a-layer	28	102
GaN/diamond	SAB + 800 °C annealing	24 nm Si + 3 nm a-layer	86	102
GaN/diamond	SAB	10 nm Si + 3 nm a-layer	53	86
GaN/diamond	SAB	2 nm Si + 2.2 nm a-layer	92	86
GaN/diamond	CVD	50 nm dielectric	21	186
GaN/diamond	CVD	50 nm dielectric	34	186
GaN/diamond	Eutectic bonding	Ti(5 nm)/Au(240 nm)/Ti(5 nm)	>100	159
GaN/diamond	SAB	1.9 nm SiO_x+0.3 nm a-layer	120	103
GaN/diamond	SAB	1.9 nm SiO_x+0.6 nm a-layer	89	103
GaN/diamond	SAB	2.0 nm SiO_x+1.1 nm a-layer	42	103
GaN/diamond	SAB	3.1 nm SiO_x+1.1 nm a-layer	29	103
GaN/SiC	MBE	none	230	84
GaN/SiC	SAB	3 nm a-SiC	169	85
GaN/SiC	SAB + 1000 °C annealing	3 nm c-SiC	229	85
GaN/SiC	CVD	5 nm SiN_x	286	174
GaN/SiC	MOCVD	~28 nm AlN	~200	187, 188
GaN/SiC	Epitaxial growth	50 nm AlN	40	189
GaN/SiC	PVD	Ti (5 nm)/AuSn (40 nm)/Ti (5 nm)	15	178
GaN/SiC	MOCVD	Not mentioned	8.3	90
GaN/SiC	LP-MOCVD	None	225	91
GaN/SiC	LP-MOCVD	15 nm AlN	250	91
GaN/SiC	LP-MOCVD	65 nm AlN	260	91
SiC/diamond	SAB	10 nm Ti + 4 nm a-layer	15	107
SiC/diamond	SAB + 1000 °C annealing	1.5 nm a-layer	60	89
SiC/diamond	SAB + 1100 °C annealing	10 nm a-SiC	150	110
SiC/diamond	SAB + 1100 °C annealing	10 nm a-SiC	111	110
SiC/diamond	SAB + 800 °C annealing	10 nm a-SiC	92	110
SiC/diamond	SAB + 800 °C annealing	10 nm a-SiC	54	110
SiC/diamond	SAB	10 nm a-SiC	38	110
SiC/diamond	SAB	10 nm a-SiC	33	110
GaN/Si	MBE	38 nm AlN	188	190
GaN/Si	MBE	38 nm AlN	128	92
GaN/Si	MOCVD	100 nm AlN	263	193
GaN/Si	PVD	Ti (5 nm)/AuSn (40 nm)/Ti (5 nm)	16.5	178
GaN/Si	MOCVD	Not mentioned	14	190
GaN/AlN	MBE	None	620	194
GaN/BAs	Plasma bonding	2 nm a-Al_2O_3	250	156
GaN/Al_2O_3	MOCVD	Not mentioned	10	195
GaN/Al_2O_3	MOCVD	Not mentioned	8.3	190
GaN/Al_2O_3	MOCVD	Not mentioned	10	196
GaN/SiO_2	CVD	Not mentioned	14	196
GaN/Zno	PVD	10–12 nm defective	490	197
GaN/Al	PVD	Not mentioned	190	198
GaN/Al	PVD	Not mentioned	92	199
GaN/Al	PVD	Not mentioned	160	195
GaN/Al	PVD	Not mentioned	47–161	192

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TABLE II. (Continued.)

Materials	Method	Interlayer	TBC (MW m^{-2} K^{-1})	References
GaN/Al	PVD	Not mentioned	400	200
GaN/Au	PVD	Ti adhesion layer	250	199
GaN/Au	PVD	Not mentioned	55	199
GaN/Cr	PVD	Not mentioned	230	198
GaN/Cr	PVD	Not mentioned	180	201
Ga_2O_3/diamond	van der Waals bonding	None	17	23
Ga_2O_3/diamond	ALD	None	179	202
Ga_2O_3/diamond	ALD	Ga-rich	136	202
Ga_2O_3/diamond	ALD	O-rich	139	202
Ga_2O_3/SiC	Smart-cut +800 °C annealing	Not mentioned	150	203
Ga_2O_3/SiC	Smart-cut	30 nm Al_2O_3+3.5 nm a-SiC	72	24
Ga_2O_3/SiC	Smart-cut +800 °C annealing	30 nm Al_2O_3+2 nm a-SiC	65	24
Ga_2O_3/SiC	Smart-cut	9.4 nm Al_2O_3+2.7 nm a-SiC	100	24
Ga_2O_3/SiC	Smart-cut +800 °C annealing	9 nm Al_2O_3+2 nm a-SiC	88	24
Ga_2O_3/SiC	SAB + °C annealing	1.5 nm defective	244	108
Ga_2O_3/SiC	Fusion bonding	15 nm SiN_x/10 nm SiO_2/15 nm SiN_x	23	160
Ga_2O_3/SiC	Smart-cut	20 nm Al_2O_3+4 nm a-layer	60	126
Ga_2O_3/SiC	Smart-cut + 900 °C annealing	20 nm Al_2O_3+4 nm 3-layer	133	126
Ga_2O_3/Au	Wedge deposition	None	45	204
Ga_2O_3/Au	Wedge deposition	2.5 nm Cr	530	204
Ga_2O_3/Au	Wedge deposition	5 nm Ti	260	204
Ga_2O_3/Au	Wedge deposition	>3 nm Ti	410	204
Ga_2O_3/Au	E-beam evaporation	Defective layer	31	205
Ga_2O_3/Ti	E-beam evaporation	Defective layer	17	205
Ga_2O_3/Ni	E-beam evaporation	Defective layer	83	205
Ga_2O_3/Al	E-beam evaporation	Defective layer	82	205
AlN/Si	Sputtering	2 nm a-layer	95	157
AlN/Si	Plasma bonding	10 nm SiO_2/AlON	105	157
AlN/SiC	Epitaxial growth	None	350	7

optical methods, the RMS roughness of the sample surface with less than 15 nm is preferred to avoid the interference of the diffusively scattered pump. However, based on the deflection instead of the intensity of the probe beam, I-TOPS has a much higher tolerance for surface roughness.[221,222]

2. 3ω method

Another well-established thermal characterization method is the 3ω method, which is an electrothermal method and does not depend on pump–probe laser system. In 3ω method, a metallic heater is deposited onto the sample's surface to induce periodic heating by applying an alternating current (AC).[223] An AC with frequency ω generates Joule heat and consequently temperature change at frequency of 2ω. The resistance change of the heater is proportional to its temperature change, resulting in a resistance change at frequency 2ω. By combining the original AC at ω, a voltage signal at 3ω is ultimately generated and measured. Varying the heating frequency allows for different temperature oscillations ΔT, enabling the extraction of thermal transport properties by fitting the temperature signal ΔT against ω. The frequency can be modulated from a few Hz to several kHz; however, a low modulation frequency leads to a deeper thermal penetration depth and reduced sensitivity to TBC compared to pump–probe methods such as TDTR. Additionally, fabrication of a metal heater on the surface is more complicated than deposition of a metal layer. For electrically conductive materials, a passivation layer is required between the heater and the sample, which further reduces the sensitivity to TBC of the buried interface.

3. Comparison

TDTR offers the highest specical resolution in depth direction, followed by FDTR and nanosecond-TTR. If the sample structure is technically optimized to maximize the sensitivity to the interface according to different charactering methods, TDTR achieves the highest sensitivity for high TBC measurements. However, the TDTR setup is the most complicated and expensive one among the discussed methods. The low modulation frequency of SSTR, I-TPOS, and the 3ω method result in large thermal penetration depths and low sensitivity to interfaces, making them more suitable for measuring the thermal resistance of a bulk material or stacked multilayers. Due to the low

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TABLE III. Comparison of different thermal characterization techniques.

	3ω	TTR	FDTR	TDTR	SSTR	I-TOPS
Heating frequency	Hz–kHz	kHz	kHz-tens of MHz	MHz	~200Hz	~100Hz
Temperature probing	Metal heater	CW laser	CW laser	Mostly femtosecond pulse[226]	CW laser	CW laser
Best spatial resolution	Tens of μm	A few μm	A few μm	1 μm	A few μm	A few μm
Thermal penetration depth	A few μm-tens of μm	A few μm-tens of μm	A few hundred nm-tens of μm	Tens of nm-A few μm	A few μm-hundreds of μm	A few μm-hundreds of μm
Sensitivity of TBC	Low	Medium	Medium-high	High	Low	Low
Sample preparation difficulty	Hard	Simple	Simple	Simple	Simple	Simple
Cost	Low	Low	Medium	High	Low	Low

thermoreflectance coefficient, TTR exhibits a lower SNR and precision. Although thermoreflectance methods are more sensitive to surface roughness, several approaches have been developed to mitigate this issue.[224,225] In contrast, the 3ω method offers better tolerance to surface roughness; however, an insulation layer may be necessary and a large area of smooth surface is still required for heater deposition. Table III summarizes different measurement techniques.

4. TBC mapping

Advanced thermoreflectance techniques have also been developed to fulfill the requirement of 2D mapping capability in the characterization of semiconductor heterostructures. A dual-modulation-frequency TDTR was developed for simultaneous mapping of thermal conductivity (κ) of semiconductor thin film and thermal boundary conductance (TBC) of the semiconductor–substrate interface. The capability is demonstrated in the measurement of a 300-nm-thick β-Ga_2O_3 film bonded with a SiC substrate,[203] as illustrated in Fig. 29. The mapping results consist of independent TDTR measurements at each location with a step size of 5 μm, closely aligning with the in-plane spatial resolution. At each location, β-Ga_2O_3 κ in Fig. 29(a) is initially derived from the TDTR ratio signal at a modulation frequency of 9.3 MHz and delay a time of 650 ps, where sensitivity to both Al/β-Ga_2O_3 TBC and β-Ga_2O_3/SiC TBC is close to zero [see Fig. 29(c)]. Subsequently, the β-Ga_2O_3/SiC TBC in Fig. 29(b) is obtained from the signal at a modulation frequency of 1.6 MHz and a delay time of 330

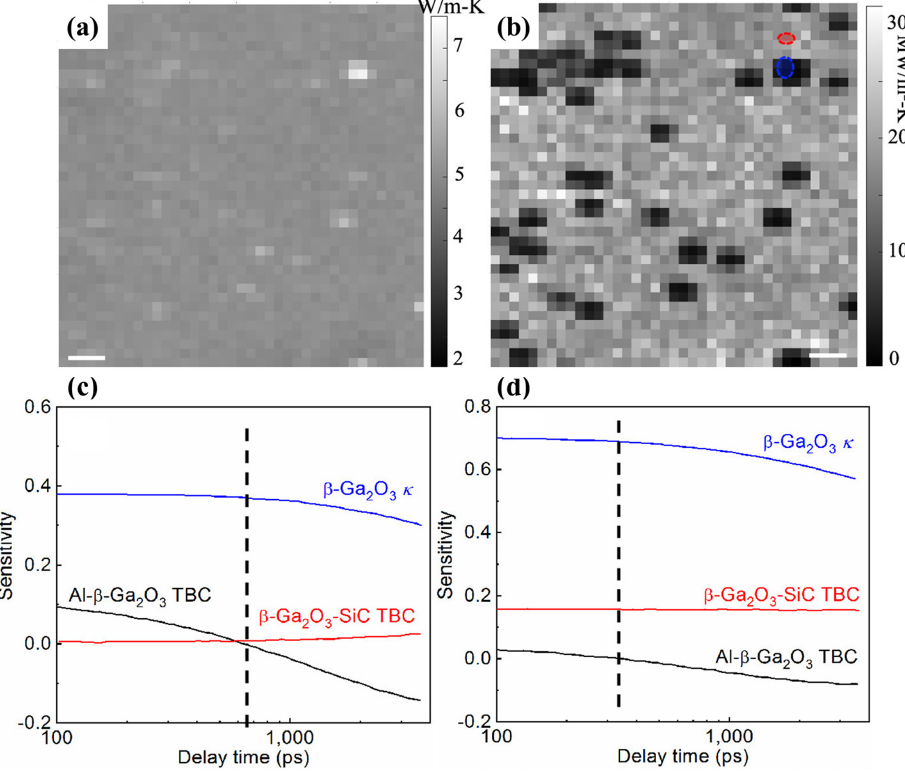

FIG. 29. Dual-modulation-frequency TDTR mapping of thermal conductivity and thermal boundary conductance for Al-coated 300 nm-thick β-Ga_2O_3 film bonded with SiC substrate and annealed in O_2. (a) The β-Ga_2O_3 thermal conductivity (κ) map was obtained from the ratio signal at a modulation frequency of 9.3 MHz and delay time of 650 ps. (b) The β-Ga_2O_3/SiC TBC map was obtained from the ratio signal at a modulation frequency of 1.6 MHz and delay time of 330 ps given the β-Ga_2O_3 κ in (a). The scale bar is 20 μm. TDTR sensitivity of Al/β-Ga_2O_3 TBC, β-Ga_2O_3 κ, and β-Ga_2O_3/SiC TBC with a modulation frequency of (c) 9.3 and (d) 1.6 MHz. Reprinted with permission from Cheng *et al.*, ACS Appl. Mater. Interfaces **13**, 31843 (2021). Copyright 2021 American Chemical Society.[203]

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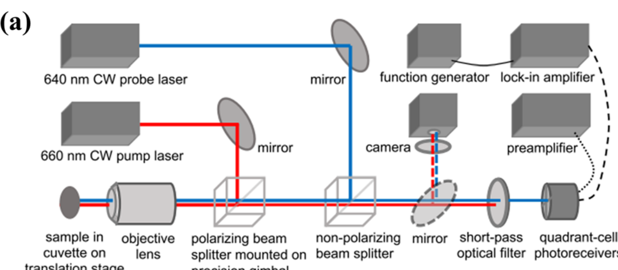

FIG. 30. TBC mapping by I-TOPS. (a) Schematic diagram of immersion thermo-optic phase spectroscopy (I-TOPS) experiment. (b) Mapping of the thermal boundary conductance of SiC–diamond interface in 98 nm Al/870 nm 3C-SiC/single-crystal diamond sample. Reprinted with permission from Sun *et al.*, Appl Phys Lett **124**, 042201 (2024). Copyright 2024 AIP Publishing LLC.[220]

ps, given the obtained β-Ga_2O_3 κ, at which sensitivity to Al/β-Ga_2O_3 TBC is zero [see Fig. 29(d)].

The TBC map in Fig. 29(b) shows a disadvantage of the smart-cut β-Ga_2O_3 thin films bonded with SiC substrates: weakly bonded area forms after high-temperature annealing, which is necessary for epitaxial growth of β-Ga_2O_3 devices.[203] As shown in Fig. 29(b), low TBC areas are observed in the directly bonded β-Ga_2O_3-SiC interfaces after annealing at 800 °C. Furthermore, study is needed to address this problem by adding an interfacial layer or improving the bonding technique.

The high SNR of I-TOPS enables TBC mapping at a high rate, and the setup of the system is shown in Fig. 30(a).[220] The mapping capability is demonstrated by mapping the thermal boundary conductance of the buried interface between 870 nm 3C-SiC and single-crystal diamond, as shown in Fig. 30(b). The thermal conductivity of SiC and the thermal boundary conductance of the Al-SiC interface are used as known parameters.

B. TBC enhancement

In this part, the discussions underscore the critical significance of TBC between the device layer and substrate. Without high TBCs, the potential benefits of utilizing substrates with high thermal conductivity remain compromised. Theoretical calculations and simulations, bonding techniques, growth methods, or interfacial engineering play indispensable roles in enhancing TBC. These provide fundamental insights into the factors, which govern heat transport across interfaces. This section introduces a series of experiments and simulations aimed at improving TBC.

The transfer of heat across a semiconductor interface can be simply treated as phonon transmission from one material to the adjacent material.[226,227] At room temperature, most transmitted phonons retain the same frequency, a process known as elastic scattering.[228] As the temperature increases, inelastic phonon transport, arising from anharmonic phonon scattering, becomes significant. This allows for the merging of two or more low-frequency phonons into one high-frequency phonon, or the splitting of a high-frequency phonon into several low-frequency phonons.[230] Consequently, the TBC of an interface is generally influenced by factors such as temperature,[231] pressure,[232] interface condition (including roughness, mixing, and contact area),[233–235] and the phonon properties of the two materials.[236] In practical applications, it is often difficult to control the temperature and pressure at the interface. However, several strategies can enhance TBC: increasing the actual contact area, modifying the atomic structure at the interface to align the DOS between the two materials, and introducing an interlayer to bridge phonon modes across the interface.

1. Contact area enlargement

Since TBC depends on the number of phonons that transmit through an interface, a larger actual contact area at the interface provides more phonon transmission and improve TBC. Cheng *et al.* engineered a patterned Si/diamond interface with various sizes of trench patterns on the Si substrate.[83] The diamond was grown on the Si substrate via graphoepitaxy. The TEM image in Fig. 31(a) illustrates the interface with clearly visible trench patterns. Three samples with no pattern, small trenches, and large trenches were fabricated for comparison, denoted as sample references A and B. Figure 31(b) displays the TBCs and thermal conductivity of the grown diamond for each interface. The results indicate that patterned interfaces tend to exhibit high TBCs. A maximum TBC enhancement of 65% can be achieved. This is attributed to the large contact area between Si and diamond in patterned interfaces, facilitating thermal transport. The increased thermal conductivity of diamond in the patterned sample is attributed to the large average grain size of diamond grown on the patterned surface, along with a preferred grain orientation perpendicular to the interface due to the impact of the pattern. This structure also enhances the quality of the diamond/silicon contact interface, where no voids were observed, thereby further improving the TBC.

Lee *et al.* focused on another structure designed for TBC enhancement.[237] Through theoretical calculation,[238] they proposed that a nanopillar array at the interface increases the effective area for phonon transport, thereby improving TBC. However, such a structure also obstructs the path of certain phonons, leading to a potential decrease in TBC. Achieving an optimal condition for TBC enhancement requires a balance in adjusting the geometric dimensions of the nanopillar array. The SEM images of experimentally achieved nanopillar arrays in different sizes are shown in Fig. 31(c).[237] The measured TBC of the patterned Al/Si interfaces confirms that the geometric size of the nanopillar indeed influences the TBC. Figure 31(d) shows the TBC comparison between a patterned interface and a planar interface at different temperatures, revealing a significantly enhanced TBC for the patterned interface with an increase in up to 88%. Zhou *et al.* further explored similar nanopatterns using detailed non-equilibrium molecular dynamics (NEMD) simulations.[235] Their findings indicate that adjusting the height, length, and apparent area of the interface allows the TBC of the Si/4H-SiC interface to be tuned over a wide range—from 300 to 1000 MW m^{-2} K^{-1}. However, no experimental work has yet been conducted to validate these predictions.

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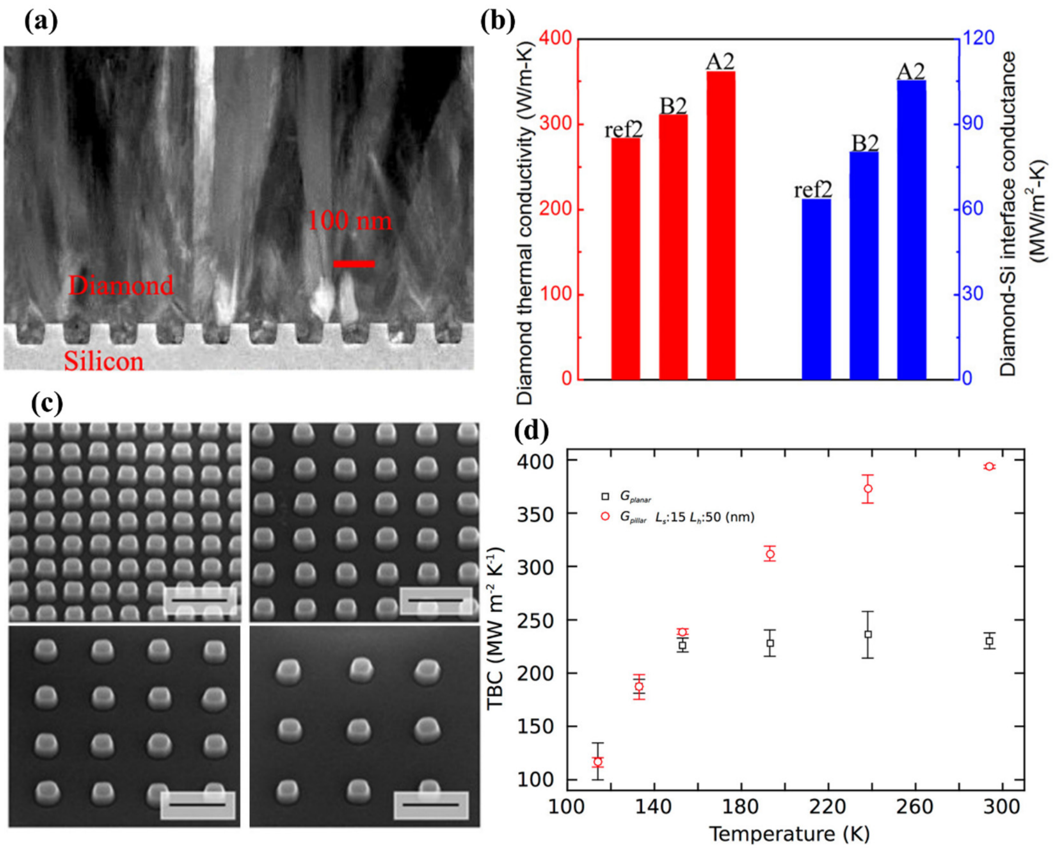

FIG. 31. The interfacial engineering for TBC enhancement. (a) The TEM image of the patterned Si/diamond interface. (b) The TBCs and diamond thermal conductivity comparison of different samples. Reprinted with permission from Cheng *et al.*, ACS Appl. Mater. Interfaces **11**, 18517 – 18527 (2019). Copyright 2019 American Chemical Society.[83] (c) The SEM images of the nanopillar structure in different sizes on the Si substrate surface. (d) The TBC comparison of the planar interface and a nanostructured interface as a function of temperature. Reprinted with permission from Lee *et al.*, ACS Appl. Mater. Interfaces **8**, 35505 – 35512 (2016). Copyright 2016 American Chemical Society.[237]

2. Interfacial engineering

Elastic phonon transport across interface only involves phonons with frequency exists in both sides, and thus, the TBC is strongly affected by the phonon frequency overlap of two materials. However, the materials we are interested in may intrinsically have distinct phonon frequency, such limitation cannot be overcome by simply enlarging the contact area. An important way to promote elastic phonon transport is to modify the atomic structure near the interface that would redistribute the phonon energy of one side to better match the other.[68,239] While these methods hold great potential, they are still challenging to implement in practice due to their involvement with sub-nanometer interface structures, such as atom substitution or ultra-thin layers of isotopes. Nonetheless, they may deepen our understanding of the microscopic mechanisms of interfacial heat transfer and pave the way for new paths in TBC enhancement.

Li *et al.* conducted molecular dynamics (MD) simulations to study light atoms doping around the GaN/SiC interface.[240] The MD simulation model is depicted in Fig. 32(a), while the results are presented in Fig. 32(b). The findings show that, when the doped skin is thin, there is a noticeable improvement in TBC, but excessively thick doped layer has a counterproductive effect. This is because while light atom doping enhances TBC, it also decreases thermal conductivity in GaN, ultimately reducing the overall thermal conductance. The mechanism of TBC enhancement is elucidated in Figs. 32(c) and 32(d), where TBC is highly correlated with the matching of phonon density of states (PDOS) on each side of the interface. The PDOS of SiC and GaN is shown in Fig. 32(c), where overlap areas appeared in the middle and high frequency regions. When light atoms are doped, the PDOS of each component are shown in Fig. 32(d). The PDOS of the light atom also overlaps with SiC and GaN in middle- and high-frequency regions. The peak of the GaN PDOS in middle frequency region also decreases due to the doping. The calculated spectral thermal conductance is shown in Fig. 32(e), and the quantum effect was also taken into consideration. In middle- and high-frequency regions, the spectral thermal conductance of the doped condition significantly increases while a slightly decrease occurs in the low-frequency region. The results are consistent with the TBC accumulation as shown in Fig. 32(e).

Except for light atom doping, Lee *et al.* also studied the introduction of isotopes to interfaces.[241] They applied non-equilibrium molecular dynamics (NEMD) calculations to study the impact of isotopes like

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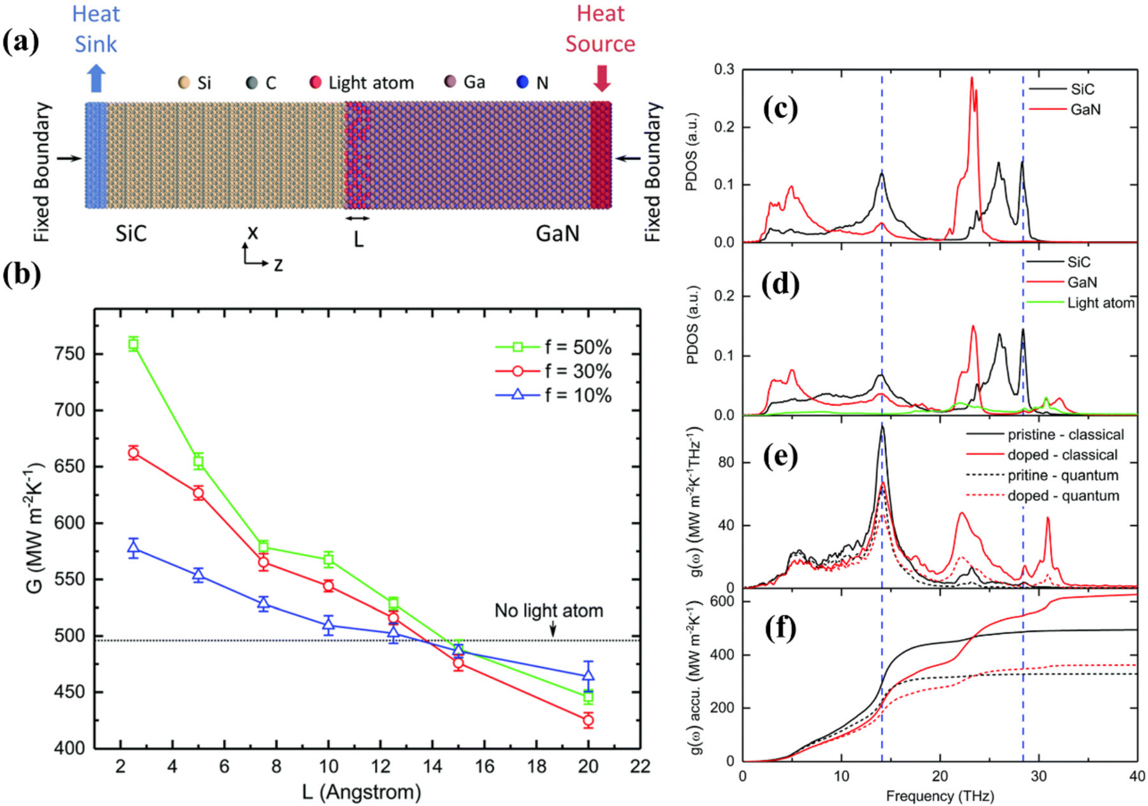

FIG. 32. The effect of light atoms on interfacial phonon transport. (a) The model used for the simulation. (b) The TBC of different concentrations of light atoms and the length of the doped region *L*. (c) The PDOS of GaN and SiC before the doping. (d) The PDOS of GaN, SiC, and the doped light atoms after the doping. (e) The calculated spectral thermal conductance obtained by different calculation methods. (f) Accumulation of thermal conductivity obtained by different calculation methods. Reprinted with permission from Li *et al.*, Phys. Chem. Chem. Phys. **21**, 17029–17035 (2019). Copyright 2019 Royal Society of Chemistry.[240]

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^{15}N or ^{71}Ga at different concentrations and with various geometrical factors, as depicted in Fig. 33(a). Figure 33(b) displays the vibrational power spectra (VPS) of the relevant elements, highlighting how ^{15}N differs from N in VPS at a low frequency. This difference enhances energy exchange between high-frequency optical phonons of GaN and low-frequency acoustic phonons of SiC through three-phonon scattering, thereby boosting TBC. Meanwhile, the added isotopes also pre-scatter the phonons and redistribute their energy, by supplement additional high-frequency phonons for scattering. Figure 33(c) shows that introducing isotopes of light atoms is highly effective in TBC enhancement. Figure 33(d) shows the impact of such introductions on the thermal conductivity of GaN, revealing a reduction due to increased phonon scattering. The isotope region should not be too far away from the interface, which prevents the phonons from being re-scattered in the bulk GaN and returning to their original states. A thin layer of isotopes near the interface is sufficient to achieve considerable TBC enhancement without a significant reduction on the overall thermal conductivity.

3. Phonon bridging

An interlayer with phonon properties compatible with both adjoining materials can serve as a bridge, facilitating phonon transport across the interface. It has been reported extensively that an interlayer can serve as a phonon bridge to enhance TBC.[243–246] Lee *et al.* reported their calculations on how to determine the optimal interlayer.[242] The schematic diagram of the simulation supercells used for NEMD calculation is shown in Fig. 34(a), along with the boundary conditions. The calculated temperature profile, as depicted in Fig. 34(b), shows two clear temperature jumps on either side of the intermediate layer. The intermediate layer is set as diatomic molecules, and the proportion of lighter atoms in total weight is defined as r_{IL}. The effects of r_{IL} on the total TBC across the intermediate layer and the related two interfaces are illustrated in Fig. 34(c). There exists an optimal r_{IL} for the TBC to reach maximum. This enhancement mechanism is related to phonon bridge. Figure 34(e) shows the VPS of GaN, SiC, and the intermediate molecule with different r_{IL} values. When r_{IL}=0.2, the VPS of the intermediate molecule overlaps with GaN and SiC simultaneously, acting as a phonon bridge to connect phonon transmission on both sides and maximizing TBC.[243–246] The intermediate material needs to have VPS, which matches GaN and SiC. AlN is a suitable candidate, as shown in Fig. 34(f). The calculated total TBC of an intermediate layer consisting of materials shown in Fig. 34(d) confirms that, if materials in Fig. 34(f) are selected as interlayers to enhance TBC of SiC/GaN interface, AlN should have the best performance.

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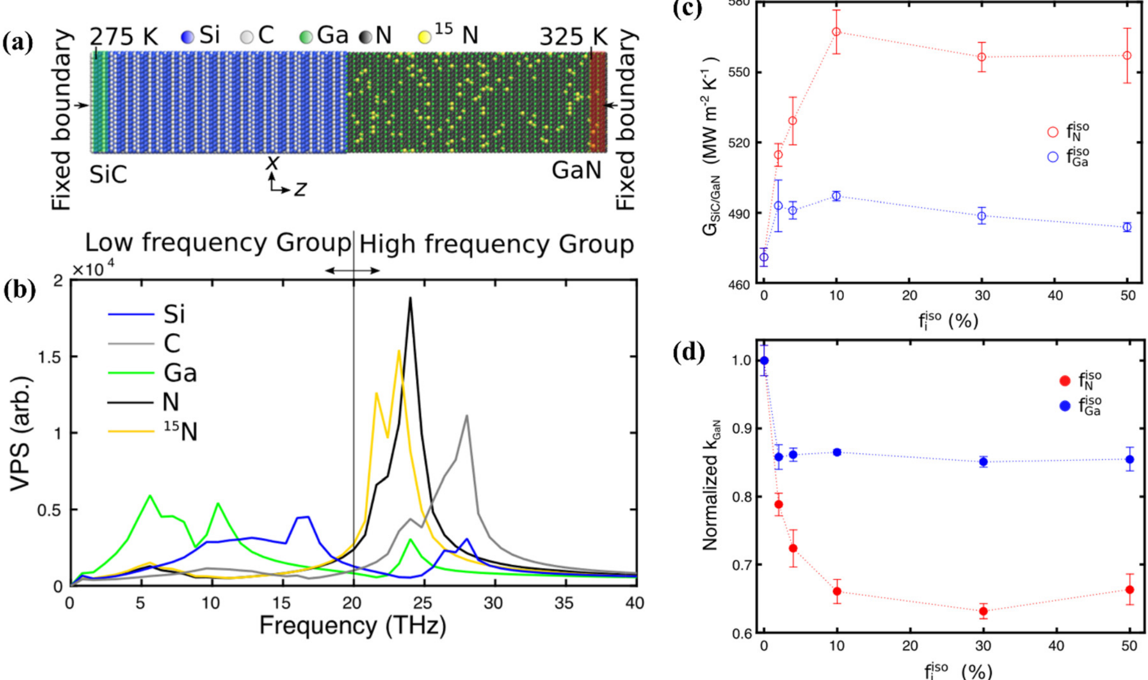

FIG. 33. The enhancement of GaN/SiC TBC by introducing isotopes. (a) The model used for MD simulation. (b) The vibrational power spectra (VPS) of different components in the system. (c) The effect of isotopes on TBC enhancement. (d) The normalized thermal conductivity of GaN as a function of the isotope concentration. Reprinted with permission from Lee *et al.*, Appl. Phys. Lett. **112**, 011603 (2018). Copyright 2018 AIP Publishing LLC.[241]

Proper treatment of the interface structure plays a crucial role in enhancing the quality of the region near the interface, allowing it to function more effectively as a phonon bridge. A high-quality region with minimal structural defects reduces phonon-defect scattering, thereby improving the overall TBC across the interface.[191] Motivated by this concept, Li *et al.* experimentally investigated the impact of AlN interlayer thickness on the TBC of GaN/SiC. Similarly, Tian *et al.* reported that introducing an amorphous SiC (a-SiC) layer has the potential to improve the TBC of AlN/SiC interfaces. Using NEMD simulations, they demonstrated that the a-SiC layer promotes inelastic phonon transport—shifting low-frequency phonons on the SiC side to higher frequencies and vice versa on the AlN side. This additional inelastic phonon transport channel enhances TBC.[247]

4. Other mechanisms

Adnan *et al.* demonstrated that TBC can be enhanced by introducing an additional interface adjacent to the original one.[248] The first interface functions as a phonon mode filter, selectively allowing only certain phonon modes to pass through. If the distance between the two interfaces is smaller than the phonon mean free path (MFP), the filtered phonons travel ballistically to the second interface, experiencing minimal scattering and retaining their original modes. When the second interface has similar phonon mode selection characteristics, TBC increases, as all phonon modes reaching it can propagate through. Moreover, replacing a sharp interface with a disordered, mixed interface can improve TBC by facilitating phonon pre-scattering and increasing the overlap of phonon DOS.[236,244] However, if interface mixing is not applied, ensuring a smooth interface is essential, as surface roughness has been shown to reduce TBC by promoting diffusive scattering.[234] Strengthening the bonding at the interface also improves TBC. As the bonding type transitions from weak van der Waals interactions to strong covalent bonds, the TBC improves correspondingly.[92,185] Naturally, if the bonding between two materials is extremely weak, they may separate, preventing thermal transport across the interface. However, further altering the bonding type at semiconductor interfaces remains challenging.

It is important to note that the aforementioned methods may not always enhance TBC. When an interlayer is added, an additional interface and additional thermal resistance are introduced, which potentially hinders thermal transport through the interface region.[178] Xu *et al.*, as referenced in Sec. III, studied the negative impact of interlayer thickness on TBC.[103] They highlighted that a significant mismatch in vDOS between the amorphous mixing layer and either the diamond or SiO_x layer can precipitate a sharp decline in TBC across the entire interface. This disparity escalates with the thickness of the interlayer. Consequently, even a slight increase in interlayer thickness precipitates a considerable reduction in total TBC, surpassing the additional thermal resistance posed solely by the thicker interlayer. Modifying atomic composition leads to increased phonon-defect scattering, resulting in large thermal resistance near the interface. Fabricating trenches to increase contact area may cause more phonons to be blocked or backscattered.[238] When a mixing layer is applied, the degree of disorder significantly affects the TBC, making it difficult to control in practice. In

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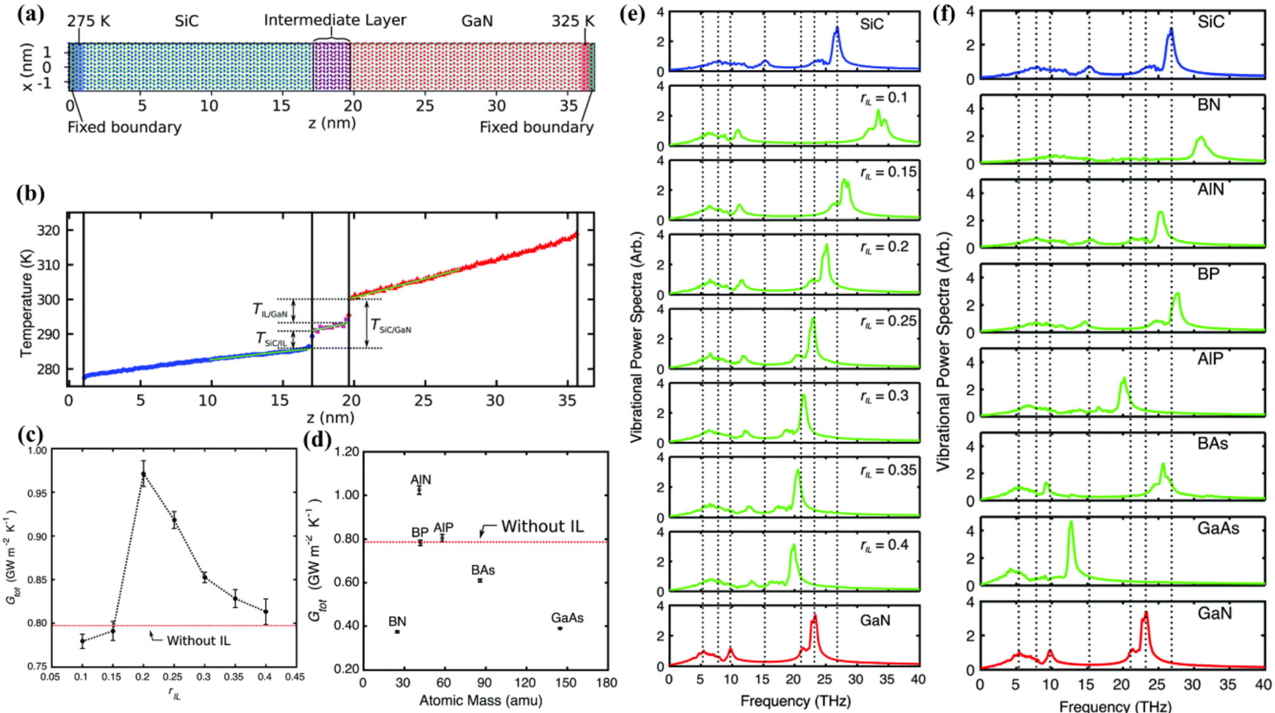

FIG. 34. TBC enhancement by applying an intermediate layer. (a) The model used for the NEMD simulation. (b) The calculate temperature profile across the interface. (c) The TBC as a function of the proportion of lighter atoms in total weight (r_{IL}). (d) The TBC across the overall interface which includes the intermediate layer. (e) The phonon VPS as a function of r_{IL}. The VPS of GaN and SiC are also added for comparison. (f) The phonon VPS of some materials. The VPS of GaN and SiC are also added for comparison. Reprinted with permission from Lee *et al.*, Phys. Chem. Chem. Phys. **19**, 18407–18415 (2017). Copyright 2017 Royal Society of Chemistry.[242]

some experiment and theory, it reduces the overall TBC.[233,244] In summary, when strategies are applied to improve TBC, the positive effects must outweigh the negative ones. However, whether a method has an overall positive impact depends strongly on the specific materials forming the interface, requiring case-by-case analysis.[4] In practice, the addition of an interlayer is the most commonly used approach, while other methods are still largely limited to theoretical research. A deeper understanding of the fundamentals of thermal boundary resistance is essential to develop methods with broader applicability and effectiveness.

C. Fundamental understanding of TBC: Interfacial phonon mode

The development of high-energy-resolution electron energy-loss spectroscopy (EELS) in a STEM enables the probing of vibrational modes with exceptional energy resolution and spatial resolution. At atomic scales, localized phonon modes near interfaces can be experimentally measured, offering insights into interfacial phenomena.[249–253] While traditional theories of interfacial thermal transport rely on phonon transmission concepts, recent molecular dynamics (MD) simulations over the past decade have revealed the presence of localized phonon modes at interfaces, acting as conduits for thermal transport. Experimental observations of these interfacial phonon modes hold the potential to elucidate and resolve this ongoing debate. In this section, we will discuss recent studies concerning the experimental detection of these interfacial modes.

Qi *et al.* employed the newly developed four-dimensional electron energy-loss spectroscopy (4D EELS) technique to investigate the interfacial phonon dispersion relation of a BN/diamond interface.[254] The experimental setup, illustrated in Figs. 35(a) and 35(b), comprised a 3D EELS with a large beam convergence angle for obtaining the PDOS and a 4D EELS utilizing a medium convergence angle to capture momentum transfer.[251] STEM images of the BN/diamond interface measured in this study are presented in Figs. 35(c) and 35(d), alongside their corresponding atomic models in Figs. 35(e) and 35(f). Figure 35(g) illustrates the measured phonon dispersion curves of BN, the interface, and diamond. Notably, the interface phonon dispersion curve deviates from a simple linear combination of the two bulk materials. By subtracting the average of the two bulk dispersion curves from the interfacial dispersion curve, as demonstrated in Fig. 35(h), negative density indicates the presence of isolated modes that impede vibration at the interface.[255] The calculated phonon dispersion curve of the localized interfacial phonon modes is depicted in Fig. 35(i), with calculation results corroborating the measured data, as shown in Figs. 35(j) and 35(k). Furthermore, Fig. 35(l) illustrates phonon vibrations near the interface, with acoustic, optical, and isolated modes identified in Fig. 35(k).

Li *et al.* conducted measurements of phonon peaks corresponding to different modes across the AlN/Si interface and AlN/Al interface, identifying the existence of localized interfacial phonon modes.[256]

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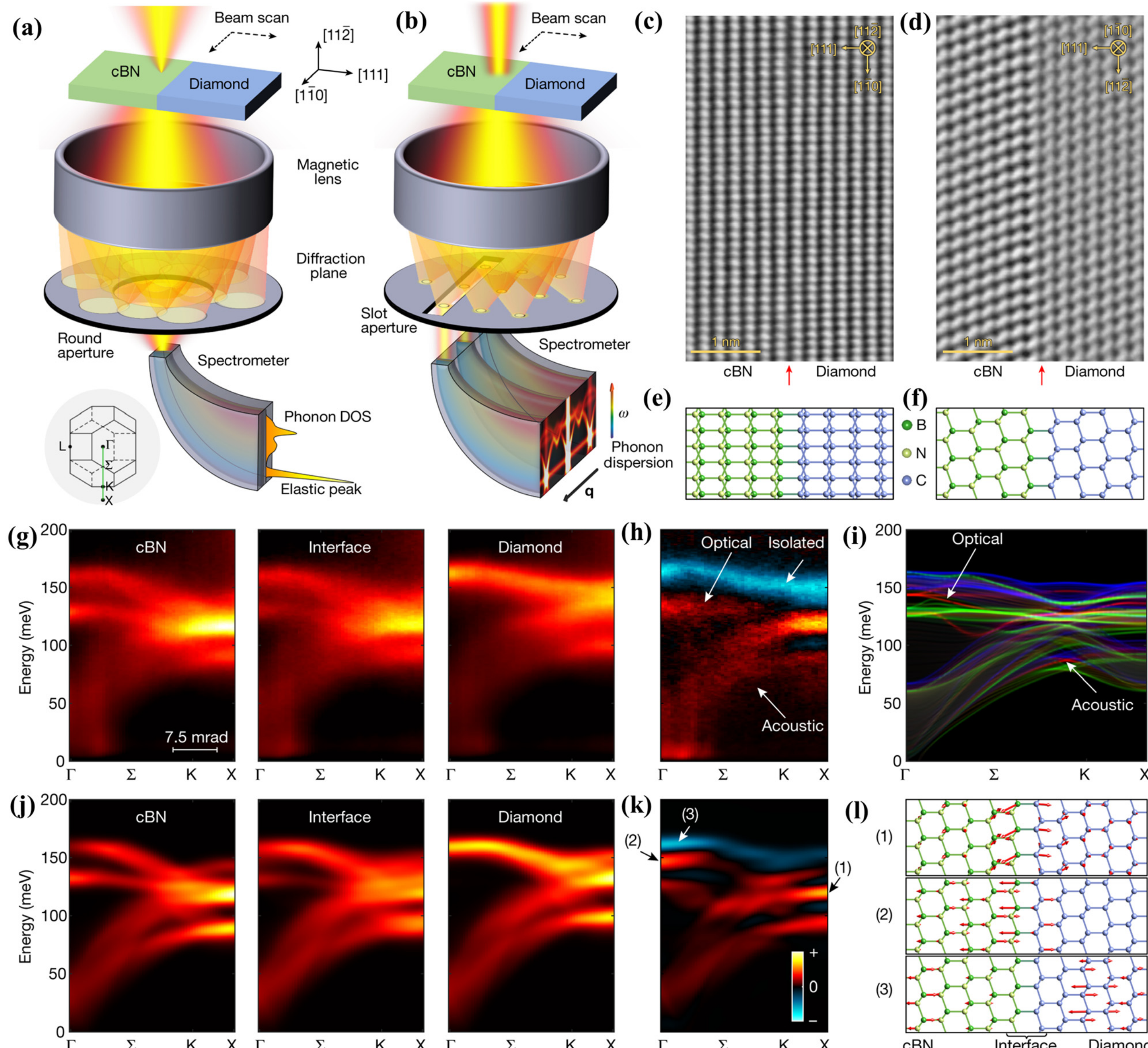

FIG. 35. The observation of interface phonon modes at the cBN/diamond interface. (a) The 3D EELS used to measure the PDOS. The inset is a bulk Brillouin zone (BZ), and the green line is the interface BZ. (b) The 4D EELS used to measure the phonon dispersion curve. (c) and (d) The STEM images of the cBN/diamond interfaces, viewed from different direction. (e) and (f) The corresponding atomic crystal structure. (g) The measured phonon dispersion curve. (h) The measured signal of the interfacial phonon modes. (i) The simulation results of the phonon dispersion curve. (j) The simulation results of the phonon dispersion curves. (k) The difference between the simulated interface curve and the average of the two bulk curves. (l) Phonon eigenvectors of three phonon modes labeled in (k). Reprinted with permission from Qi *et al.*, Nature **599**, 399–403 (2021). Copyright 2021 Springer Nature.[254]

The atomic-resolution high-angle annular dark field (HAADF) image in Fig. 36(a) shows the structure of the AlN/Si interface, together with the structure model. Figure 36(b) shows the phonon peaks of AlN/Si interface. Different peaks represent different phonon modes in the bulk or near the interface. The calculation results are shown in Fig. 36(c). The LA1/TO1 mode in the Si shift to a lower energy and connect with the TA2 mode in AlN which is shifted to a higher energy. As a result, a phonon bridge is formed. The TO1 mode in Si and the TO3 mode in AlN are similar to well. Such phonon bridge is accomplished by extended phonon modes, and the TA1 mode of the Si which penetrates into the AlN side corresponds to the localized mode. On the contrary, such phonon bridge does not exist in AlN/Al interface, which is shown in Fig. 36(d). The phonon peak mapping across such interface by EELS is shown in Fig. 36(e), and the calculation results are

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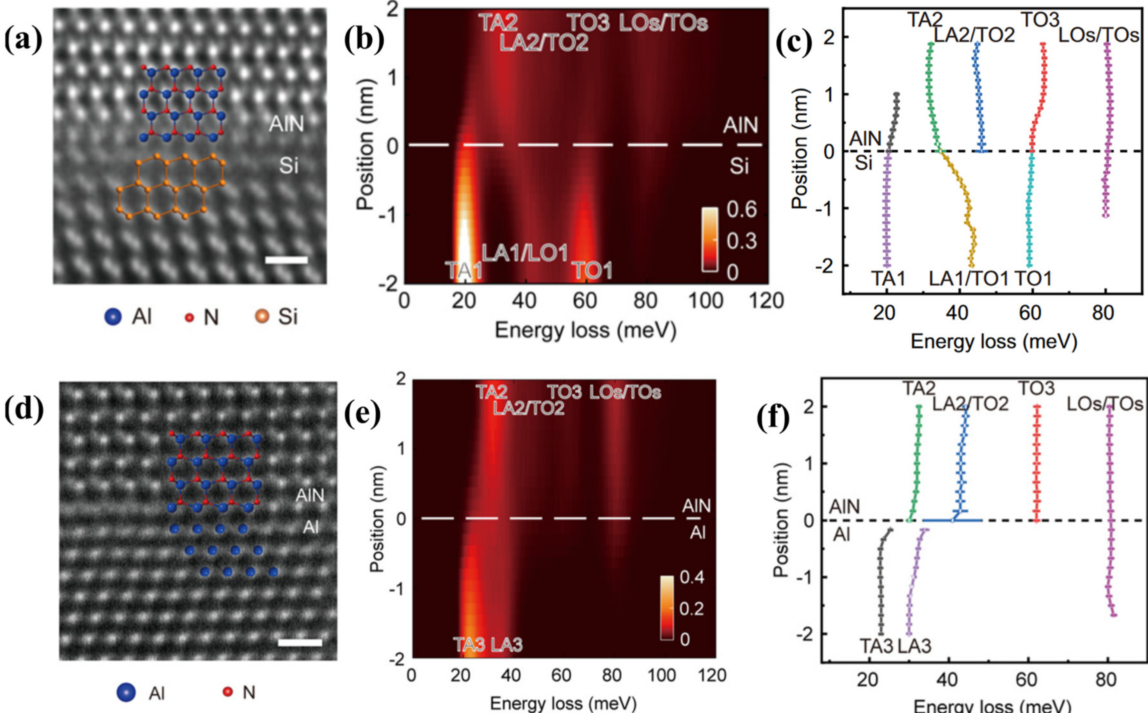

FIG. 36. The interfacial phonon modes at the nitride interfaces. (a) The atomic image and the model of the AlN/Si interfacial structure. (b) EELS mapping across the AlN/Si interface. (c) The calculated phonon peaks of different phonon modes across the AlN/Si interface. (d) The atomic image and the model of the AlN/Al interfacial structure. (e) EELS mapping across the AlN/Si interface. (f) The calculated phonon peaks of different phonon modes across the AlN/Al interface. Reprinted with permission from Li *et al.*, Proc. Natl. Acad. Sci. U. S. A. **119**, e2117027119 (2022). Copyright 2022 National Academy of Sciences.[256]

shown in Fig. 36(f). No phonon bridge was formed, and some of the modes disappear before they reach the interface, like TA3 and LA3 in Al.

Localized phonon modes across Si/Ge interfaces were also experimentally observed by Cheng *et al.*[257] The schematic diagram of the EELS measurements is presented in Fig. 37(a), involving electron beam sweeping through a path across the interface to measure vibrational spectra. EELS results in Fig. 37(b) show distinct EELS signals at the interfacial region compared to the bulk materials. Individual vibrational spectra of the three regions are shown in Fig. 37(c), indicating unique spectra for Ge, Si, and the interface. The spectral peak at the interface around 12 THz cannot be obtained by linearly combining the spectra of Ge and Si, suggesting the existence of a localized phonon mode. Figure 37(d) confirms a weak peak around 12 THz at the interface, affirming the presence of a localized phonon mode at approximately 12 THz. Furthermore, molecular dynamics (MD) simulation results reveal a peak in the PDOS at the intermixing region which are not attributed by Ge or Si, further supporting the existence of interfacial phonon modes.

V. DEVICE-LEVEL SIMULATIONS AND DEMONSTRATIONS

This section amalgamates TBC within an entire electronic device or structure to provide a more intuitive assessment of the cooling efficacy across different heterostructures. It integrates simulation outcomes alongside experimental data, showcasing the full potential of heterostructure-based cooling methodologies.

A. Thermal simulations of devices

The heterostructures discussed above influence the peak temperature or temperature distribution of electronic devices. This section delves into simulations of temperature distributions in electronic devices, aiming to estimate the effects of heterostructures, interfaces, and materials on device cooling. Finite element simulations and analytical solutions provide convenient solutions for calculating temperature distribution in electronic devices, particularly for those devices that are challenging to measure directly.

In practical electronic devices, the multi-finger structure is frequently utilized for MOSFETs, although thermal crosstalk may arise when the gate pitch is too narrow. Yuan *et al.* explored the temperature distribution of a β-Ga_2O_3 MOSFET employing bottom-side cooling without a specific high thermal conductivity substrate.[258] The channel temperature profile across the lateral direction is shown in Fig. 38(a). The channel temperature profile across the lateral direction is depicted in Fig. 38(a), revealing that the maximum channel temperature increases as the gate pitch narrows, accentuating thermal crosstalk and signifying heat accumulation from each gate without dissipating into the substrate.[259,260] Conversely, employing only one finger mitigates thermal crosstalk, as illustrated in Fig. 38(b). As the gate pitch increases, the maximum channel temperature approaches that of the

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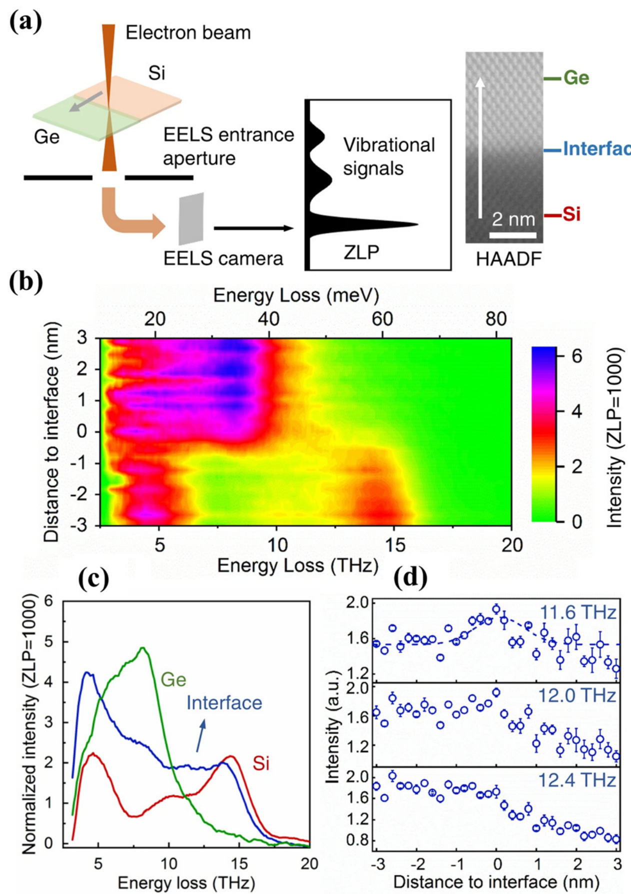

FIG. 37. The observation of localized interfacial phonon mode at Ge/Si interface. (a) The schematic diagram of the EELS mapping. The inset is the STEM image of the interface. (b) The line scanning of the vibrational spectra across the interface. (c) Vibrational spectra measured by EELS of the three regions. (d) The EELS intensity of different vibration frequencies across the interface around 12 THz. Reprinted with permission from Cheng *et al.*, Nat. Commun. **12**, 6901 (2021). Copyright 2021 Springer Nature.[257]

single-finger configuration. Additionally, Guo *et al.* simulated the temperature distribution of a GaN/diamond device using COMSOL Multiphysics.[101] The temperature profile, displayed in Fig. 38(c), indicates thermal crosstalk, with higher temperatures observed in channels nearer to the center. The inset further discusses the effect of interfacial thermal resistance (the reciprocal of TBC) on temperature distribution, emphasizing its significant impact on peak temperature.

Cheng *et al.* computed temperature distributions of power devices based on analytical solutions and estimated the impacts of TBCs and substrate materials.[90] The model structure and geometric dimensions utilized for the calculations are shown in Fig. 39(a). The model structure and geometric dimensions used for the calculations are depicted in Fig. 39(a), with the temperature profile of a GaN-on-SiC device shown in Fig. 39(b). By employing a GaN/SiC TBC of 170 MW m^{-2} K^{-1}, analytical solutions for the maximum temperature rises of GaN and β-Ga_2O_3 devices are presented in Figs. 39(c) and 39(d), respectively. The thermal performance of both GaN and β-Ga_2O_3

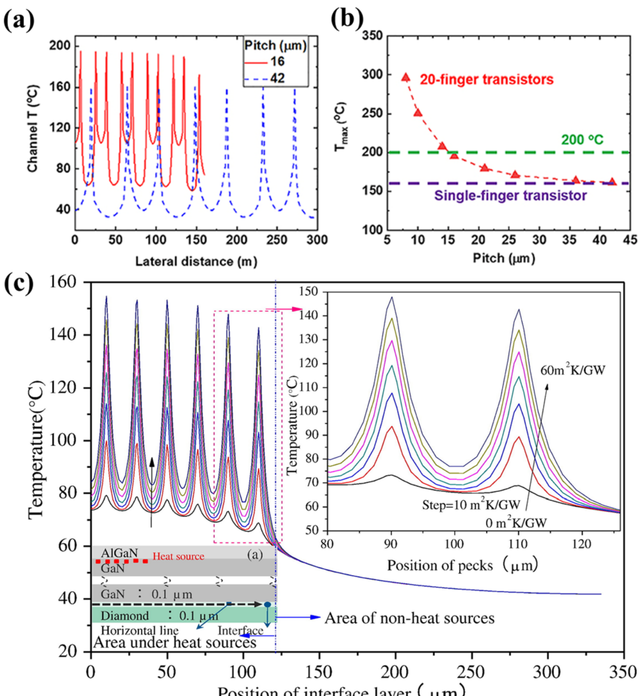

FIG. 38. The finite element simulation results of the multi-finger devices based on β-Ga_2O_3 and GaN/diamond. (a) The thermal crosstalk effect of different finger pitches. (b) The comparison of the 20-finger device and the single-finger device. Reprinted with permission from Yuan *et al.*, J. Appl. Phys. **127**, 154502 (2020). Copyright 2020 AIP Publishing LLC.[258] (c) The temperature distribution underneath the GaN/diamond device surface with different GaN/diamond TBCs. The inset displays the impact of different GaN/diamond TBCs on peak channel temperature. Reprinted with permission from Huaixin Guo *et al.*, Diamond Relat. Mater. **73**, 260–266 (2017). Copyright 2017 Elsevier.[101]

devices significantly improved when utilizing composite substrates, such as β-Ga_2O_3/SiC, compared to conventional substrates. Similar studies have been conducted by Cheng *et al.*[23,86] and Anaya *et al.*,[261] highlighting the advantageous effects of employing composite substrates.

Moreover, the utilization of composite substrates, such as β-Ga_2O_3-SiC, markedly reduces the temperature of a β-Ga_2O_3 device.[160] The structures of the β-Ga_2O_3 device on a β-Ga_2O_3 substrate and the β-Ga_2O_3 device on a modified β-Ga_2O_3-SiC composite substrate are illustrated in Figs. 40(a) and 40(b). Integration of β-Ga_2O_3 and SiC is achieved through the fusion bonding technique. The structure of the multi-finger device is depicted in Fig. 40(c), alongside the location of the maximum temperature. Figures 40(d) and 40(e) display the maximum temperature rise of single-finger and six-finger β-Ga_2O_3 devices, revealing a substantial improvement in thermal performance through the use of composite substrates, achieving up to 2 to 3 times the power density. Especially for multi-finger devices, where thermal crosstalk occurs and heat accumulates, the enhancement of cooling performance becomes particularly significant. A similar conclusion was drawn by Song *et al.*,[262] who not only explored the use of SiC but also simulated an ideal design by substituting the β-Ga_2O_3 substrate with single-crystalline diamond, demonstrating even better thermal

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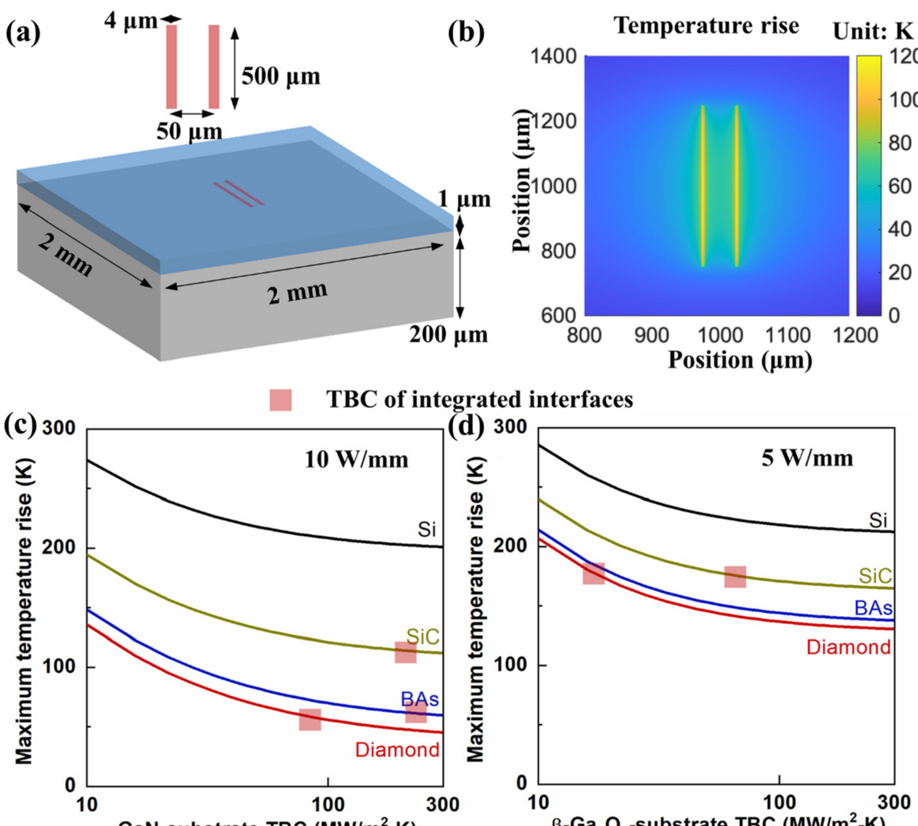

FIG. 39. The effects of TBC and substrate materials on the max channel temperature rise. (a) The model used for max temperature calculation based on analytical solution. (b) The surface temperature distribution of a GaN-on-SiC device. (c) The maximum temperature rise of a GaN device as a function of different substrates and TBC. (d) The maximum temperature rise of a β-Ga_2O_3 device as a function of different substrates and TBC. Reprinted with permission from Cheng *et al.*, Appl. Phys. Lett. **120**, 030501 (2022). Copyright 2022 AIP Publishing LLC.[90]

performance under optimized conditions. Additionally, they studied the transient thermal response of these structures, finding that the ideal structure with a single-crystalline diamond substrate reached maximum temperature under a power pulse much faster than the SiC substrate (~4 vs ~300 μs).

Various thermal designs, such as incorporating high thermal conductivity materials at different locations within the device or adopting flip-chip packaging methods, can yield different cooling performances. However, not all strategies are readily feasible through experiments. Finite element simulations play a crucial role in assessing the feasibility and cooling performance of these strategies, providing valuable guidance for future device designs.

In addition to substituting the substrate with high thermal conductivity materials such as diamond and SiC, other cooling strategies can be applied to GaN or β-Ga_2O_3 devices.[258,264–267] These cooling techniques can primarily be categorized into three methods: bottom-side cooling, top-side cooling, and double-side cooling. Bottom-side cooling, rooted in the original design of a device, involves attaching a high thermal conductivity substrate to extract heat from the bottom of the device. The TBC between the device and substrates is critical for heat spreading. Top-side cooling, however, overcomes this drawback by directly extracting heat from the top side of the transistor. This approach can be achieved by integrating high thermal conductivity materials onto the top side of the device or through a packaging technique known as "flip-chip," wherein the die is packaged upside down to connect the heat sink directly to the top side of the device, a method already utilized for thermal management.[268,269] The double-side cooling method combines the heat dissipation paths of both bottom-side and top-side cooling, which is promising for excellent thermal performance.

Shoemaker *et al.* compared the cooling performance of these different strategies through finite element simulations.[263] Figure 41(a) illustrates the schematic diagram of traditional bottom-side cooling, utilizing a high thermal conductivity substrate. Figure 41(b) depicts a diamond-incorporated flip-chip cooling strategy, employing diamond carrier and diamond passivation layer to achieve top-side cooling. Additionally, air jet impingement cooling[270] on the SiC and diamond substrates were also included in the simulation. The cooling performance is shown in Fig. 41(c). Under the condition that maintaining all devices at a maximum temperature of 200 °C, the output power density of the diamond-incorporated GaN-on-SiC device with flip-chip packaging was found to be the highest among the four methods. Furthermore, the same flip chip GaN-on-SiC method exhibits the minimum temperature rise, as depicted in Fig. 41(d), aligning with the cooling effect shown in Fig. 41(c). Figures 41(e) and 41(f) display the temperature distribution of the GaN-on-SiC device and the flip-chip GaN device, revealing significantly lower temperature with the flip-chip method.

Shoemaker *et al.* reported a reduction in total junction-to-package thermal resistance at various stages. Three cooling techniques—

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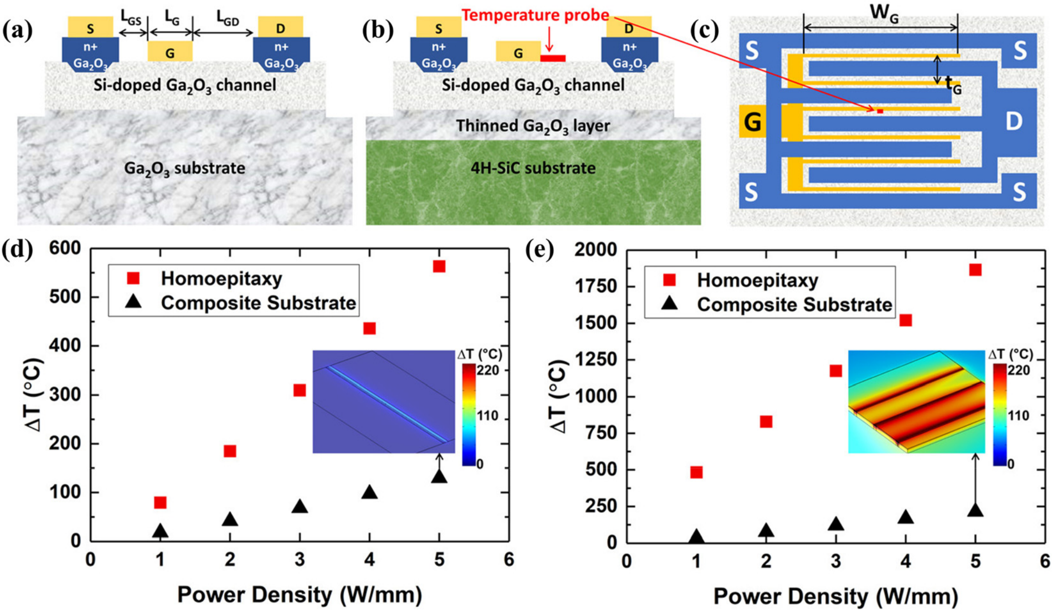

FIG. 40. The cooling effect of the β-Ga_2O_3-SiC composite substrate. (a) The diagram of the β-Ga_2O_3 device. (b) The diagram of the β-Ga_2O_3 device grown on composite substrate. (c) The layout of a multi-finger device and the location of peak temperature. (d) The temperature rise of the single-finger device with different power densities and substrates. (e) The temperature rise of a six-finger device with different power densities and substrates. Reprinted with permission from Song *et al.*, ACS Appl. Mater. Interfaces **13**, 14 (2021). Copyright 2021 America Chemical Society.[160]

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bottom-side cooling, top-side cooling, and double-side cooling—were evaluated.[282] To enhance top-side cooling performance in the double-side cooling configuration, an Au thermal bump was introduced between the diamond carrier and the top side of the device. The temperature rise of the GaN-on-SiC device under different cooling strategies was analyzed. The impact of the diamond passivation layer appeared limited, mainly due to the thinness and relatively low thermal conductivity of the polycrystalline diamond films, as well as the TBC at the diamond-device interfaces. The reduction in junction-to-package thermal resistance at different stages was quantified, with the introduction of the thermal bump yielding the most significant improvement, followed by the use of a diamond carrier.

The TBCs of GaN/diamond are low due to mismatches in phonon density of states. Another high thermal conductivity material, BAs, stands out as a promising candidate for addressing GaN hotspot problems. Wu *et al.* employed NEMD to compute the TBC between GaN and BAs. The simulation model, depicted in Fig. 42(a), incorporates a temperature curve across the structure generated by a neural network potential (NNP). Figure 42(b) presents the calculated GaN/BAs TBC as a function of temperature, with one experimental value included for comparison.[156] Figure 42(c) elucidates why the GaN/BAs interface exhibits such high TBC: the matching phonon PDOS facilitates elastic phonon transport across the interface without frequency alteration. As depicted in Fig. 42(d), the authors construct a cubic composite (50% GaN grain and 50% BAs grain) and calculate the intrinsic thermal conductivity of GaN and BAs. By applying a specified heat flux, temperature profiles [Fig. 42(e)] and heat flux distributions [Fig. 42(f)] can be determined. Figure 42(g) illustrates the overall effective thermal conductivity as a function of grain size with different combinations of GaN and BAs. When grain size is small, grain boundaries scatter all phonons uniformly. However, as grain size increases, intrinsic phonon–phonon scattering starts to dominate. Ultimately, when grain size significantly exceeds the phonon mean free paths of GaN and BAs, the size effect diminishes, and effective thermal conductivity reach a plateau. The high thermal conductivity of BAs and high TBC of GaN-BAs facilitates the near junction of GaN devices. However, one of the main challenges to use BAs as thermal management materials is the difficulty in growth of large high-quality crystals.

B. Experimental demonstrations of device cooling

This section delves into device demonstrations that measured the temperature distribution of devices with the aforementioned heterostructures, alongside an introduction to the temperature measurement technique of thermoreflectance imaging.

Many temperature measurements rely on thermoreflectance, a widely employed method known for its high spatial and temperature resolutions.[273–275] The underlying principle of thermoreflectance imaging is that the reflectivity of a material changes linearly with temperature. The coefficient of thermoreflectance (C_{th}) quantifies this relationship, enabling the identification of temperature changes by measuring variations in reflected power combined with the material's C_{th}. As an optical method, thermoreflectance imaging can map temperature profiles across the entire device, providing powerful and high-resolution temperature data, leading to its widespread adoption.[276–279] However, thermoreflectance imaging fails to measure temperature in areas inaccessible to light. The following examples mainly rely on thermoreflectance imaging.

In addition to top-side cooling, the sides of the devices can also serve as important heat dissipation paths, such as the all-around

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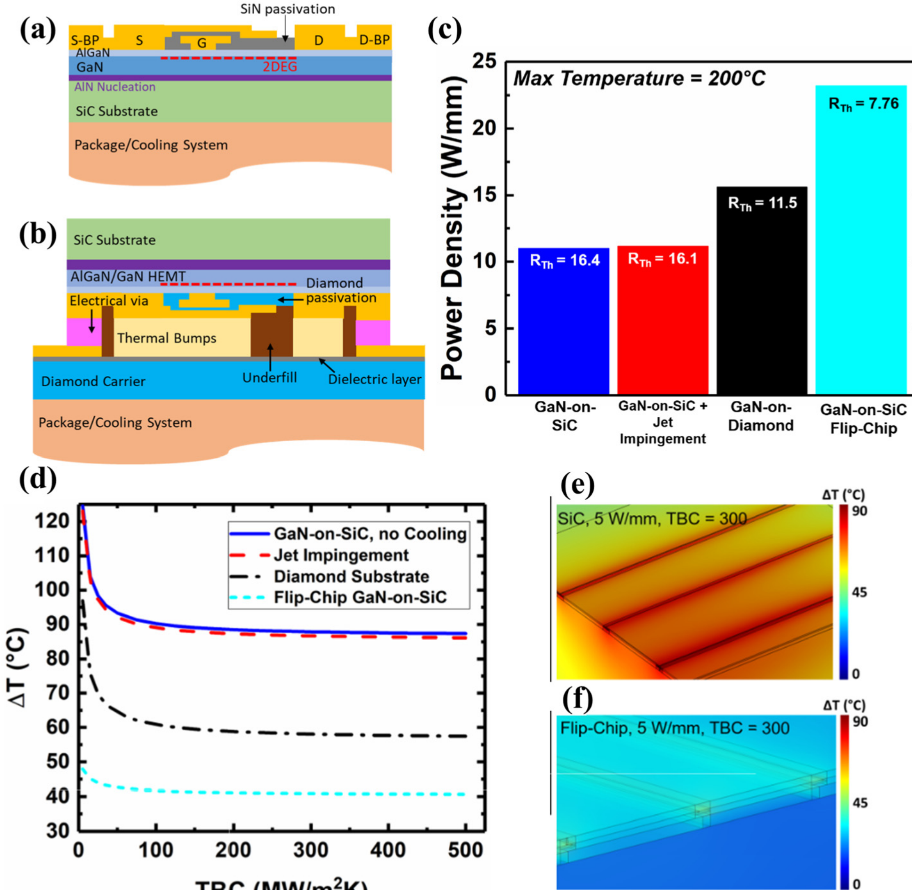

FIG. 41. The cooling effect of different cooling strategies. (a) The schematic diagram of the bottom-side cooling structure (b) The schematic diagram of the diamond-incorporated flip-chip cooling strategy. (c) The achievable power density of different cooling structure with the same maximum temperature of 200 °C. (d) The maximum temperature rise as a function of TBC between GaN and substrates with different cooling strategies. (e) The temperature profile of the GaN-on-SiC device. (f) The temperature profile of flip-chip GaN device. Reprinted with permission from Shoemaker *et al.*, IEEE Trans. Electron Devices **70**, 5036–5043 (2023). Copyright 2023 IEEE.[263]

diamond design.[281] This method involves covering nearly the entire transistor with polycrystalline diamond, aiming for optimal cooling efficiency. The fabrication process, depicted in Fig. 43(a), entails covering the whole transistor except for three electrodes with polycrystalline diamond. Recent advancements in low-temperature polycrystalline diamond growth have facilitated this strategy, producing near-isotropic high thermal conductivity diamond with minimal damage to electronic devices.[282] Temperature measurements of this device were conducted through thermoreflectance imaging and gate resistance thermometry (GRT). Figure 43(b) shows the thermoreflectance results for a control sample without a diamond layer and an all-around diamond sample at various power densities. The all-around diamond sample demonstrated a more uniform temperature distribution even at high power densities. The control sample exhibited a less uniform temperature distribution and obvious hot spots. GRT results indicated a remarkable temperature reduction of about 100 °C in the all-around diamond sample compared to the control sample under a power density of 9 W/mm. This enabled the all-around diamond sample to sustain twice as much power density as the control sample at the same maximum temperature.

Masten *et al.* adopted a top-side cooling approach by capping a 100-nm-thick nanocrystalline diamond (NCD) layer on a β-Ga_2O_3 device.[283] The device structure is illustrated in Fig. 44(a). Thermoreflectance imaging results [Fig. 44(b)], comparing the diamond-capped sample with an uncapped reference sample, revealed a halved temperature rise across the entire measurement area for the diamond-capped device, underscoring the efficacy of top-side cooling. The temperature rise as a function of power density [Fig. 44(c)] further emphasized the excellent thermal performance of the diamond-capped device. Compared to the reference sample, the diamond-capped sample could withstand nearly twice the power density with the same temperature rise. Overall, it can achieve a 42% reduction in thermal resistance by applying this method.

Kagawa *et al.* examined the surface temperature profile of GaN/3C-SiC/diamond devices.[95] As depicted in Figs. 45(a)–45(c), replacement of the substrates led to a significant temperature decrease, particularly noticeable at high power densities. The cooling performance of the GaN/SiC/diamond devices is better than the GaN-on-SiC devices while the cooling performance of the GaN-on-SiC device is better than the GaN-on-Si devices. Figure 45(d) shows the relation of temperature rise and power density. The slope for the Si substrate is nearly four times as large as that of the diamond substrate, highlighting the critical role of substrate material in cooling effectiveness.

Additionally, Helou *et al.* investigated the thermal performance of GaN devices by fabricating five GaN HEMTs on different substrates, including membrane, silicon, SiC, diamond, and SiC with a NCD

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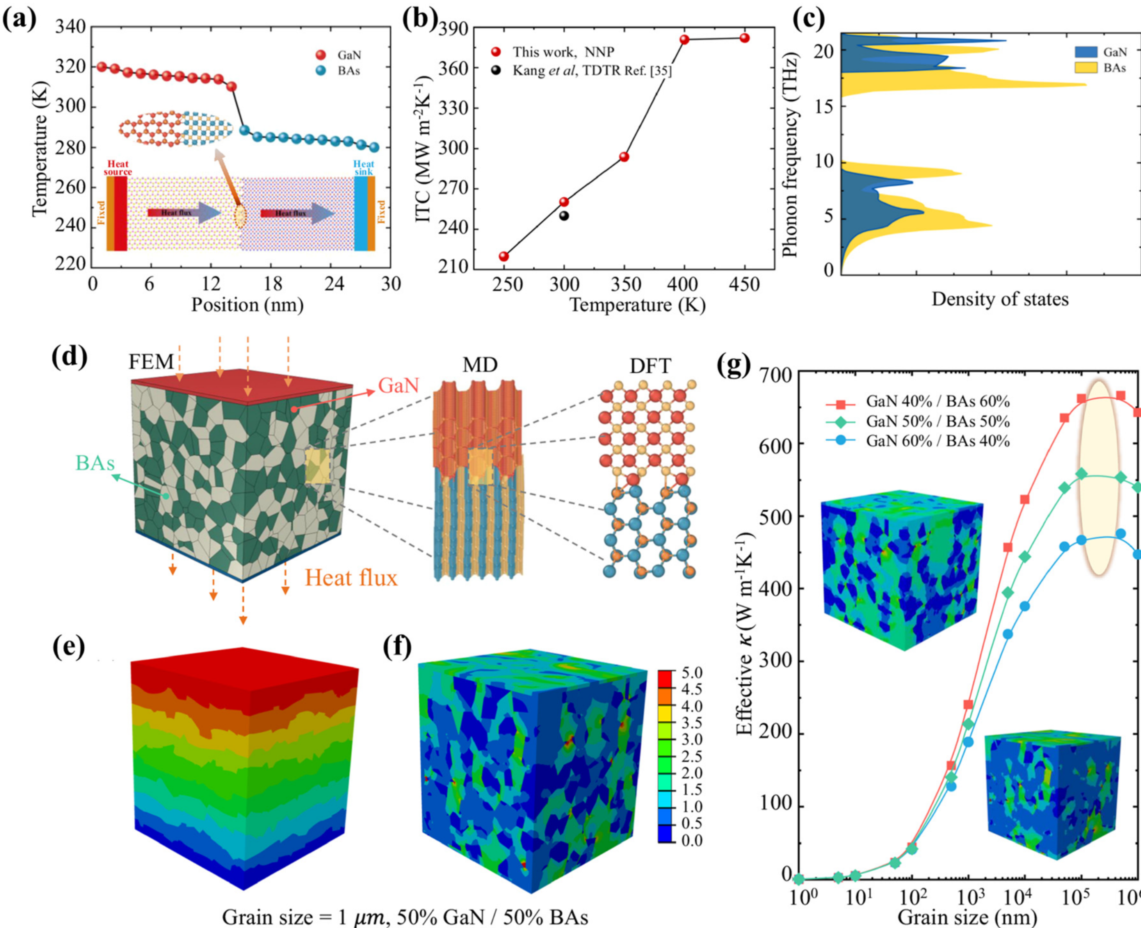

FIG. 42. The multiple scale calculations of the GaN-BAs heterostructure. (a) The simulation model of MD and the temperature distribution across the GaN/BAs interface. (b) The calculated and measured TBC of GaN/BAs interface. (c) The phonon density of states of GaN and BAs. (d) The model used to calculate thermal property of the GaN-BAs heterostructure. (e) The calculated temperature distribution of the GaN-BAs heterostructure. (f) The calculated heat flux distribution of the GaN-BAs heterostructure. (g) The effective thermal conductivity over the GaN-BAs heterostructure as a function of grain size with different combinations of GaN and BAs. Reprinted with permission from Wu *et al.*, Nat. Commun. **15**, 2540 (2024). Copyright 2024 Springer Nature.[272]

capping layer.[284] Thermoreflectance imaging was employed to measure temperature profiles across the device surface. Notably, using a diamond substrate proved to be the most effective cooling solution, while the addition of the NCD capping layer had minimal impact, contrary to earlier findings. This discrepancy is likely due to the low TBC associated with diamond integration. These results align with simulation data from Ref. 271, which suggest that the diamond passivation layer contributes only marginally to device cooling. Similarly, Tadjer *et al.* fabricated four GaN HEMTs on various silicon and diamond substrates, mapping the temperature profiles at different power densities using thermoreflectance imaging.[285] Even at high power densities, the diamond substrate demonstrated significantly superior cooling performance compared to silicon, highlighting the effectiveness of bottom-side diamond cooling.

Kang *et al.* demonstrated the integration of BAs substrates with GaN devices for near-junction cooling.[156] Due to the excellent matching of phonon density of states of BAs and GaN, the TBC of GaN-BAs interfaces are expected to be higher than the GaN–diamond interfaces. Figure 46(a) shows a top view of the GaN-on-BAs device, while Fig. 46(b) elucidates its cooling performance. Temperature measurements in this study were conducted via Raman spectroscopy near the grain side. Despite diamond has higher thermal conductivity than BAs, the cooling potential of the diamond substrate is hampered by the low TBC of the GaN/diamond interface. This work underscores the importance of TBC, which can rival the thermal conductivity of the thermal management material itself. The combination of high thermal conductivity BAs and high GaN-BAs TBC may lead to the excellent cooling performance of GaN-on-BAs device.

VI. CHALLENGES AND PERSPECTIVES

To ensure a satisfactory median device lifetime, it is essential to maintain the channel temperature of GaN electronics below 225 °C. To optimize the performance of GaN electronics and operate close to the electronic limit of GaN materials, substantial reductions in thermal

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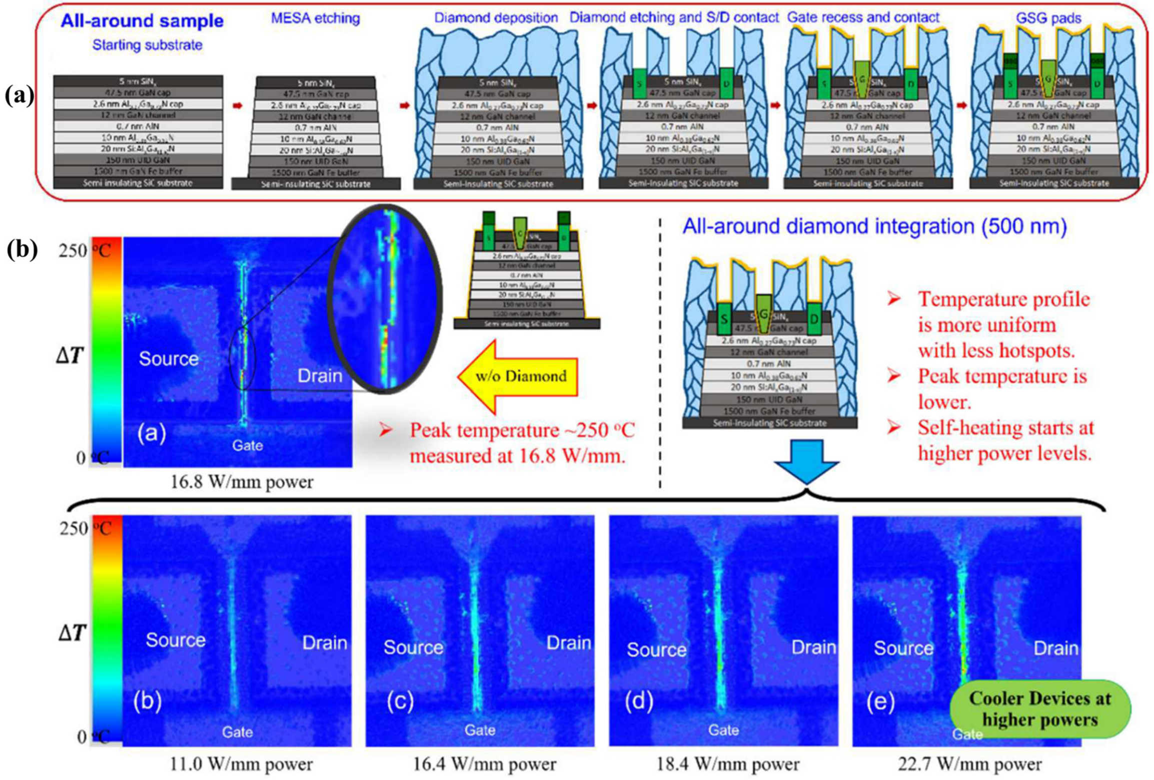

FIG. 43. The all-around diamond cooling of GaN devices. (a) The fabrication process of the all-around diamond devices. (b) The actual temperature difference between a GaN device with all-around diamond integration and a device without any diamond layer. Reprinted with permission from Soman *et al.*, 2022 International Electron Devices Meeting (IEDM). Copyright 2022 IEEE.[280]

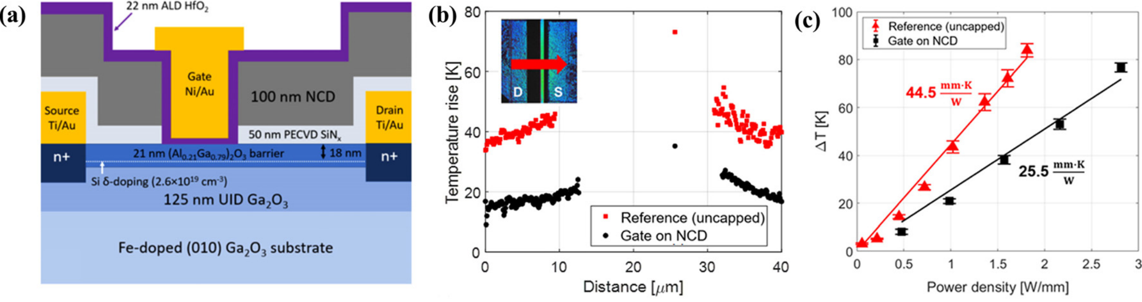

FIG. 44. Top-side cooling of a β-Ga_2O_3 device. (a) The schematic diagram of the device. (b) The temperature across the whole channel of a reference sample and a diamond-capped sample measured by thermoreflectance imaging. (c) The temperature rise of the reference sample and diamond-capped sample as a function of power density. Reprinted with permission from Masten *et al.*, Appl. Phys. Lett. **124**, 153502 (2024). Copyright 2024 AIP Publishing LLC.[283]

resistances in GaN electronics are required. It is crucial to concurrently consider the thermal resistances of semiconductor heterostructures both inside and outside the functional components of the electronics. Modifications aimed at reducing thermal resistances in functional components should not compromise electrical performance. For instance, eliminating the AlN transition layer in the epitaxial growth of GaN on SiC can reduce thermal resistance within GaN electronics. However, it introduces more defects and dislocations, leading to the degradation of electrical performance. Below, we outline several challenges and potential research directions to advance (ultra)wide bandgap semiconductor heterostructures for improved electronics cooling.

Growing high thermal conductivity materials: One potential direction to enhance the heat dissipation of GaN or β-Ga_2O_3 devices is to enhance the thermal conductivity of these materials. However, since the GaN crystal quality is already high, enhancing material quality by

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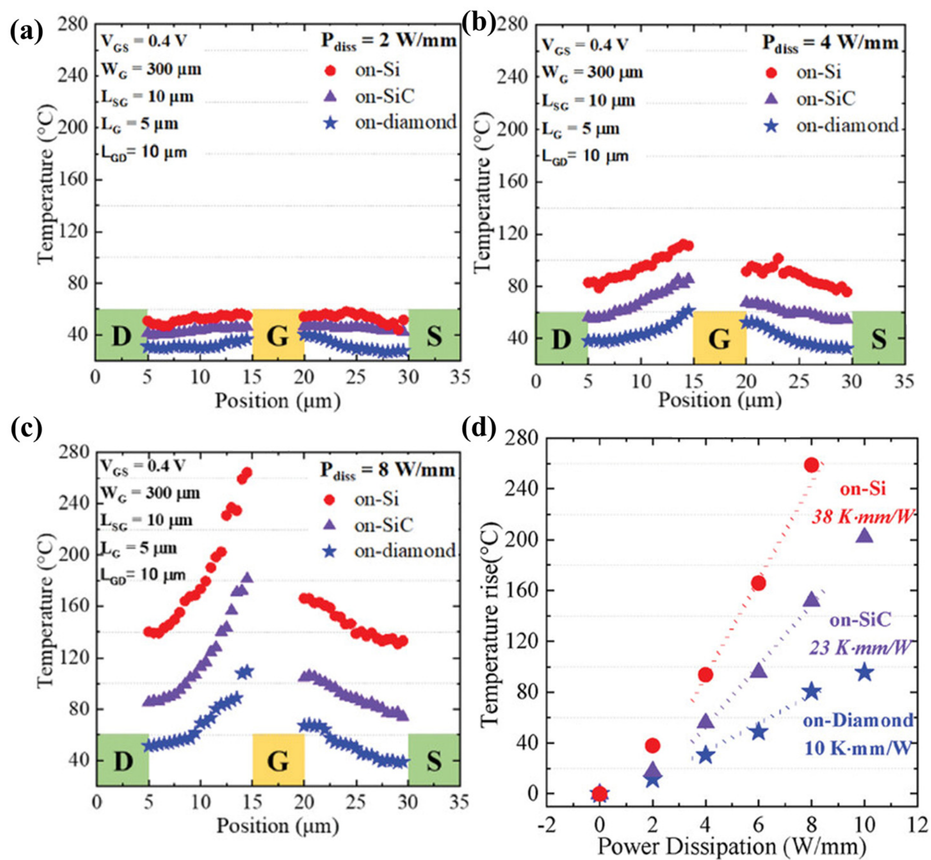

FIG. 45. The cooling effect of a GaN/3C-SiC/diamond device. (a)–(c) The surface temperature of the device with different power densities and different substrates measured by Raman thermometry. (d) The temperature rise of the devices on different substrates as a function of power density. Reprinted with permission from Kagawa *et al.*, Small **20**, 2305574 (2023). Copyright 2023 Wiley-VCH Verlag.[95]

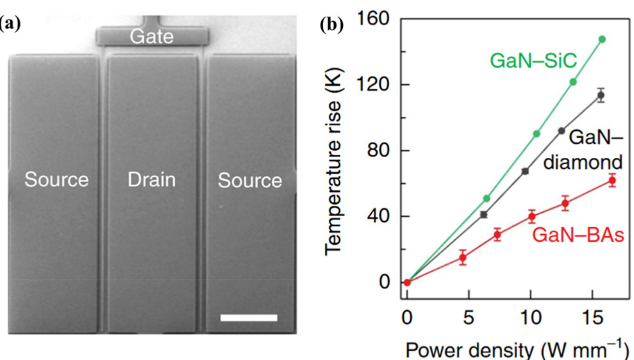

FIG. 46. The cooling performance of GaN-on-BAs devices. (a) The picture of the GaN-on-BAs device. (b) The relation between temperature rise and power density of the GaN-BAs device, compared with GaN-on-SiC and GaN-on-diamond devices. Reprinted with permission from Kang *et al.*, Nat. Electron. **4**, 416–423 (2021). Copyright 2021 Springer Nature.[156]

reducing defects, dislocations, and misfits may not significantly boost thermal conductivity. Instead, purifying the isotopes can lead to further improvement in thermal conductivity. Naturally occurring Ga consists of approximately 60% ^{69}Ga and 40% ^{71}Ga isotopes, while N is predominantly made up of 99.6% ^{14}N and 0.4% ^{15}N. These isotopes introduce mass disorder in the crystal, hindering phonon thermal transport. Theoretical calculations have shown that enriching (purifying) the Ga and N isotopes can enhance the thermal conductivity of GaN by ~65% to ~400 W m^{-1} K^{-1} near room temperature, which is comparable to SiC.[286] However, experimental measurements have only demonstrated minor improvement, likely due to residual isotopes and other impurities such as Al and oxygen in the crystals.[6] Furthermore, improvement in isotope purity of GaN materials could result in a significant enhancement in GaN thermal conductivity, especially crucial for the thermal management of vertical GaN devices. Neither experimental nor theoretical studies on the effects of isotope enrichment on the thermal conductivity of β-Ga_2O_3 have been reported yet. Still, considering the much more extensive phonon–phonon scattering than phonon–isotope scattering in β-Ga_2O_3, isotope enrichment is expected not to impact the thermal conductivity much.

Tantalum nitride finds extensive use in interconnects as a diffusion barrier and insulating layer within metal interconnects. Recent theoretical calculations propose that θ-phase tantalum nitride has a thermal conductivity nearing 1000 W m^{-1} K^{-1} near room temperature. This arises from a substantial frequency gap between acoustic and optical phonon modes, impeding three-phonon processes, and the semimetal's very low electron density of states near the Fermi level, resulting in weak electron-phonon scattering.[287,288] However, the experimentally measured thermal conductivity of θ-TaN is only 90 W m^{-1} K^{-1}, attributed to the nanocrystalline nature of the crystals.[289] To

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enhance the thermal conductivity of θ-TaN, the synthesis of large single crystals with a low concentration of vacancies becomes imperative. Achieving this would elevate the thermal conductivity of θ-TaN, ultimately reaching its intrinsic thermal conductivity.

An emerging avenue in microelectronics is the CMOS-compatible low-temperature growth of high thermal conductivity materials, transcending traditional substrate-side cooling to explore top-side cooling or cooling electronics post-fabrication. For instance, high thermal conductivity dielectric materials grow on the back-end-of-line or the top surface of GaN HEMTs. For the next-generation ultra-high-density integration of transistors, backside power delivery moves power supply interconnections to the backside. To fabricate vias through Si substrate, the Si substrate needs to be thinned down to about 10 μs. The heat spreading capability of the original thick Si substrate needs to be compensated by growing high thermal conductivity materials and connecting to heat sinks. The challenge lies in reconciling the conflict between low-temperature growth and maintaining high quality, essential for achieving elevated thermal conductivity. Beyond AlN and diamond, a broader exploration of materials is required to grow high-quality and high thermal conductivity heterostructures. To fully harness high thermal conductivity, the grown interfaces are equally pivotal to possess high TBC values. An ideal material should exhibit properties such as low-temperature growth, high thermal conductivity, dielectric characteristics, excellent chemical stability, vapor growth facilitating gap filling, outstanding adhesion with other electronic materials, affordability, a good match in thermal expansion coefficients, and more.

Enhancing TBC by heterogeneous integration: Replacing multiple transition layers with bonding stands out as a promising strategy for mitigating thermal resistances. Bonding techniques such as surface-activated bonding, hydrophilic bonding, and plasma bonding play a crucial role in integrating semiconductors with high TBC. However, achieving reliable bonding demands ultra-smooth surfaces with sub-nanometer root mean square (RMS) roughness, as highlighted in studies.[86,156,290,291] Challenges arise when dealing with high thermal conductivity materials like diamond, known for its exceptional hardness. Polishing such materials, particularly polycrystalline diamond, involves the intricacies of chemical–mechanical polishing (CMP). The polishing rates for different crystal orientations of diamond are variable, leading to varying grain polishing rates in polycrystalline diamond and making it challenging to obtain a large-area smooth surface for wafer bonding. Moreover, post-processes such as epitaxial growth of functional layers and annealing of metal contacts require high temperatures, raising concerns about the stability of the bonded interface. The susceptibility to de-bonding at high temperatures due to chemical instability or mismatched thermal expansion coefficients further complicates matter. Overcoming these challenges demands continuous advancements in bonding and polishing techniques.

Enhancing TBC in GaN devices emerges as a potent strategy for reducing total thermal resistances. However, TBC at heterointerfaces is strongly dependent on interfacial structure, which poses challenges in both fundamental understanding and engineering techniques.[229,231,292] The fundamental energy carrier transport mechanisms near the interfaces are still not fully understood, making it challenging to pinpoint the most effective approaches for enhancing TBC. Possible strategies such as phonon bridge, isotope engineering, chemical bonding, and ion implantation require extensive investigation. Moving this field forward necessitates collaborative efforts among researchers in thermal science, materials growth, and materials characterizations.

Phonon filtering in heterostructures: Recent theory suggests that thermal conductivity of thin films and TBC of interfaces strongly depend on the environment near them. In electronics, multiple layered structures dominate the active parts in microelectronics and power/RF electronics. The phonon transport in an individual layer are strongly affected the phonons in the adjacent layers. The phonon filtering effect can be used to tune the thermal conductivity of thin films and TBC in electronics. This filtering or coupling effect has rich physics when applying them to (ultra)wide bandgap semiconductor heterostructures.

Heterointerfaces in chiplets: Chiplets have recently garnered significant attention as Moore's law approaches its limits, and the 3D integration of chips including (ultra)wide bandgap electronics presents a substantial challenge for effective heat dissipation.[293] To ensure reliable performance, it is imperative to comprehensively understand and characterize thermal transport within chiplets while implementing proper electro-thermal co-design of the floorplan. Advanced interconnect techniques play a vital role in reducing Joule-heat generation. The development of novel dielectric materials with high or low thermal conductivity becomes essential for efficiently conducting or isolating heat within chiplets. For instance, thermal insulation between memory and logic dies is crucial. The integration of subsets or dies introduces additional interfaces, necessitating a deep understanding and optimization of interfacial thermal resistances. Proper arrangement of subsets with varying heat generation rates and the introduction of fluid pumping through microchannels within chiplets are potential technical strategies for effective thermal management. All these involve heterointerfaces, encompassing both grown interfaces and bonded interfaces. Insufficient TBC leads to large temperature differences near the interfaces, resulting in large thermal stress. Both thermal and mechanical factors simultaneously cause reliability problems.

Hybrid bonding serves as a key technique in chiplets integration, employing two distinct bonding mechanisms: oxide–oxide hydrophilic bonding and Cu-Cu thermocompression bonding. The uniformity of bonding quality in hybrid bonding remains an open question. While small unbonded areas in the oxide–oxide part may not severely impact electrical interconnection, they can significantly impede heat dissipation, leading to unnecessary localized hotspots. There is a growing demand for nondestructive techniques to characterize these bonded interfaces.

Device cooling strategies: The integration of materials has been extensively studied while the device-level integration are much less studied. Research on either device-first or bonding-first demonstrations need further study. The corresponding cooling performance needs to be estimated accurately with further improved temperature measurement techniques with high spatial and temperature resolutions. The effects of heterogeneous integration on the electrical properties needs to be accessed. The reported data about the reliability of the integrated interfaces or devices are rare, which calls for further exploration. New cooling strategies or new device layout are on demand for the increased need of heat dissipation. The combination of device-level cooling and packaging-level cooling may bring in new solutions for future high-power devices.

3D thermometry: The temperature distributions inside integrated devices are critical for device reliability and performance. Due

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to the complicated device structures, it is difficult to measure the temperature inside the electronics nondestructively. This is especially true for devices with multiple metal films which block optical access. Therefore, 3D thermometry techniques such as x ray, nuclear magnetic resonance, electron spin resonance, and acoustic techniques are on demand but need further developed.

Thermal characterizations: Accurately measuring temperature in devices with high spatial, time, and temperature resolutions is crucial yet challenging due to strongly non-uniform temperature distributions and heterogeneous thermal properties in electronics. The presence of boundaries, doping, defects, and dislocations in materials decreases thermal conductivity, while multiple-layer structures introduce thermal boundary resistances. Therefore, studying the structure–property relations of new semiconductor materials becomes essential. In this context, accurate characterizations of thermal properties with high spatial resolution are critical. Transient/*in situ* thermal measurements, along with visualization of thermal properties, are necessary for effectively characterizing electronics. A continued commitment to improving thermal measurements is indispensable for the advancement of electronics.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors declare no competing interest.

Author Contributions

Zhe Cheng: Conceptualization (lead); Funding Acquisition (equal); Writing/Original Draft Preparation (equal). **Zifeng Huang:** Writing/Review & Editing (equal); Writing/Original Draft Preparation (support). **Jinchi Sun:** Writing/Review & Editing (equal); Writing/Original Draft Preparation (support). **Jia Wang:** Writing/Review & Editing (support). **Tianli Feng:** Writing/Review & Editing (support). **Kazuki Ohnishi:** Writing/Review & Editing (support). **Jianbo Liang:** Writing/Review & Editing (support). **Hiroshi Amano:** Writing/Review & Editing (support). **Ru Huang:** Writing/Review & Editing (support).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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